HIGH-ORDER LINEARIZING PULSEWIDTH MODULATOR FOR THREE-PHASE POWER CONVERTERS

BY

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A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

2000

ACKNOWLEDGMENTS

I would like to express my deepest gratitude to my research committee chairman, Dr. Khai D. T. Ngo, for welcoming me to the power electronics group at the University of Florida. He provided constant support and encouragement for my study and research. I learned not only the knowledge of power electronics, but also a work attitude that has greatly reshaped my career. I also wish to thank Dr. Dennis P. Carroll, Dr. Alexander Domijan, Dr. Vladimir A. Rakov, and Dr. Loc Vu-Quoc for their participation on my research committee.

I am very grateful to American Research Corporation for its financial support and projects, and also Texas Instruments for a TI fellowship.

My special thanks go to my colleagues, Jun Xu and Paiboon Nakmahachal, for their helpful discussions and suggestions in my project and dissertation.

There is no word for me to describe my gratitude to my wife, Yin Xie, who spent her time taking care of our family when I was working at the lab day and night. Without her help and patience, I would not know how to finish my research and dissertation.

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August 2000

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Major Department: Electrical and Computer Engineering

The feasibility of using an analog pulsewidth modulator (PWM) to linearize balanced three-phase converters is investigated in this dissertation. Prototype circuits, models, and analysis techniques are developed.

Most balanced three-phase PWM converters that are controlled by the conventional analog PWMs have nonlinear relationships between the control and output voltages/currents. This study shows that these nonlinear relationships can be linearized by an analog high-order linearizing pulsewidth modulator (LPWM) that makes the output voltage track the control voltage linearly. Instead of multipliers/dividers, the high-order LPWM uses only integrators with the reset, and sample/holds to compute the switching instants for the switches in the converter. The inputs to the integrators of the LPWM are just linear functions of the control and state variables, but are nonlinear functions

when other analog PWMs, such as feed-forward PWMs and one-cycle controllers, are used.

The analog high-order LPWM is synthesized from switching-function averaging (SFA) equations of the three-phase PWM converter. Thanks to the SFA model of the PWM switch, the derivation of SFA state-space equations of the converter is simply done by inspection and application of definition of circuit elements, Kirchhoff's law, and other electrical principles without probing into topological details of the converter. The set of SFA equations can be transformed into an equivalent circuit in the stationary coordinates to make simulation more efficient.

In order to analyze three-phase converters that are controlled by the LPWM or other pulsewidth modulation techniques, all three-phase component models in the rotating coordinates, including PWM switches, sources, and passive components, are developed. After three-phase components are replaced by their models in the rotating coordinates, the time-variant three-phase circuit is transformed into a time-invariant equivalent circuit that makes analysis and design much easier. The model of the high-order PWM is also developed. It is useful to analyze the LPWM-controlled converter and evaluate time delay caused by sampling effects.

The synthesis and analysis theories of the high-order LPWM are verified by a 1 KW prototype of a three-phase boost inverter. Both simulation and experimental results agree with the analysis. The experimental results show that the control circuit is simple, and the output voltages of the inverter can

track the control voltages linearly, and they have low-distortion sinusoidal waveforms.

In summary, the synthesis and analysis techniques are developed for linearization of a three-phase boost inverter in the dissertation. As general methods, they can be applied to other three-phase topologies, multi-phase or multi-level converters.

CHAPTER 1
INTRODUCTION

With the development of high-speed, high-power semiconductors, the switching power converter has gradually replaced linear power amplifiers to become the main power conversion product on the market. The switching power converter not only provides more efficient power conversion than the linear power converter, but also has more flexible control capability that allows the converter to meet various power demands and requirements. Therefore, research on switching power converters has received much attention. A major research issue is the linearization of switching power converters that makes the controlled variable track the control signal and improve the performance of the converter.

A basic switching power converter consists of two sections, as shown in Figure 1-1. The first section is called the power stage that usually consists of semiconductor switches and energy storage components. The power stage receives the unregulated energy from the utility power line or power converters and provides the regulated energy to customer loads. The second section is the modulator that provides control signals to the power stage.

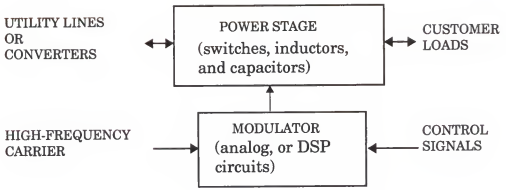


Figure 1-1 A basic switching power converter.

The modulator can be implemented by analog and digital means, depending on the requirements, complexity, and costs in converter design. The digital modulator is used mostly in three-phase converters since it has more computation capability. However, when the switching frequency is increased by size and weight requirements, the digital modulator will be limited by its clock speed. Meanwhile, when the reference voltage does not change smoothly, the sample/hold circuit with the digital modulator would be restrained by resolution. In contrast, the analog modulator is much faster, and it can handle any frequency, limited only by the capability of power stage [1].

A conventional pulsewidth modulator (PWM), as shown in Figure 1-2, consists of a comparator, a ramp carrier signal v_{rmp}, and a control signal v_c. The carrier signal provides high-switching frequency to the control signal and to the switches in the converter. The control signal is followed by the controlled variables, such as output voltages. In the conventional PWM, the carrier signal has a constant slope. The control signal is compared with the

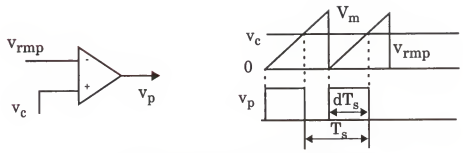


Figure 1-2 A conventional PWM.

carrier signal through the comparator. The output pulse v_p (also called switching function), generated by the comparator, is used to drive the switch in the converter. It has the duty ratio of

$$d = \frac{v_c}{V_m} \tag{1.1}$$

where V_m is the amplitude of the ramp v_{rmp}.

The output signal v_p determines the switching patterns of the converter. The controlled variable of the converter, such as the output voltage, is the function of the converter input and duty ratio of v_p that is determined by Equation (1.1). Therefore, the controlled variable of the converter can be regulated by adjusting the control signal.

The power stage in Figure 1-1 could be the dc-dc converter in the dc power conversion or the three-phase converter in three-phase ac power conversion. The most popular dc converters are shown in Figure 1-3. The conversion ratios between the output and input voltages are listed in Table 1.1. The single-phase converters and dc converters with the transformer isolation are

not listed here, because they can be derived from these basic topologies and have one independent control variable like basic dc converters.

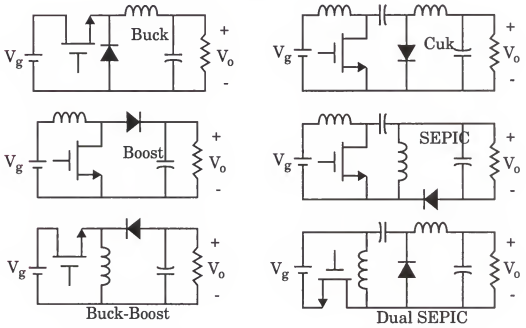


Figure 1-3 Basic dc-dc converter topologies.

Table 1.1 Voltage conversion ratios.

Converter Topology	Voltage Conversion Ratio, V_o/V_g
Buck	D
Boost	1/(1-D)
Buck-Boost	-D/(1-D)
Cuk	-D/(1-D)
SEPIC	D(1-D)
Dual SEPIC	D/(1-D)

The dc converters are used mostly in delicate and low-power applications, such as computers and microprocessors. The three-phase PWM converters are usually used in rugged, high-power applications, such as active filtering [2], UPS [3], VAR compensation [4], power generation [5], motor drives [6, 7], and multi-level converters [8]. The most popular three-phase PWM converters [9] are shown in Figure 1-4. The voltage conversion ratios

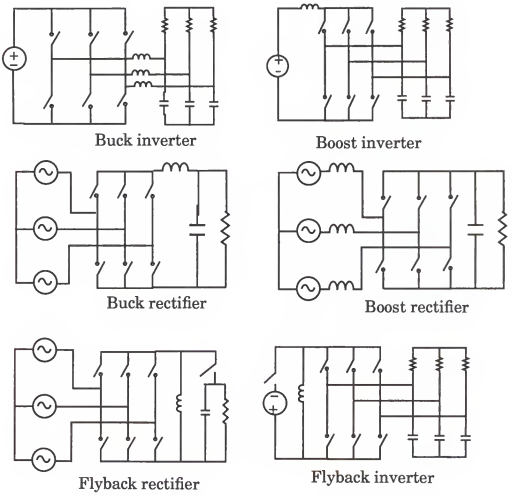


Figure 1-4 The three-phase inverters and rectifiers.

V_m/V_g are listed in Table 1.2, where V_m is the amplitude of the output voltages; V_g is the amplitude of the input voltages. The conversion ratios in Table 1.2 are derived from the balanced three-phase converters, and the input voltage and current are assumed in phase in the rectifiers. In the table, D_m is the amplitude of the sinusoidal control signal. D is the duty ratio of the dc switch in the flyback topology. It should be noted that these conversion ratios are derived by assuming that the impedance of input/output reactive components are small at input/output frequency and can be neglected.

Table 1.2 Voltage conversion ratios V_m/V_g.

Converter Topology	Inverter	Rectifier
Buck	$D_m/2$	D_m
Boost	$1/D_m$	$2/D_m$
Flyback	D/D_m	D/D_m

Although PWM converters are the most popular in various power conversions, they have an inherent problem: nonlinearity. It keeps the output voltage from tracking the control signal, gives rise to waveform distortion, and degrades the performance of the converter. The reason that generates the nonlinearity can be found by investigating the voltage conversion ratios of PWM converters in Table 1.1 for dc converters, in Table 1.2 for three-phase converters, and duty ratios shown in Equation (1.1). The conventional PWM with a constant slope carrier produces a linear relationship between the duty ratio and the control signal as shown in Equation (1.1). When the duty ratio is used

to control nonlinear converters that have a nonlinear relationship between the duty ratio and the output voltage, as shown in Table 1.1 and Table 1.2, the output voltage is proven to be a nonlinear function of the control voltage.

The nonlinear problem of PWM converters has been solved mainly by the small-signal linearization technique of negative feedback control. Recently, large-signal PWM linearization techniques were proposed in [10] and [11]. As an alternative linearization technique, the large-signal PWM linearization features an open-loop, steady-state linear control-to-output relationship, regardless of operating conditions, leading to simple and stable control circuit design. Moreover, this technique has better line voltage regulation not only for the linear converters, but also for the nonlinear converters that are difficult for the feed-forward control [12].

The large-signal PWM linearization techniques in [10, 11] can successfully solve the nonlinear problem for dc-dc converters and single-phase inverters, in which the PWM controller deals only with a single control variable. However, three-phase converters or multi-phase converters have more than one control variable. Therefore, the first-order PWM linearization is limited in three-phase converters or multi-phase converters. Nevertheless, the idea of the large-signal linearization is a useful concept that could be extended to the three-phase converters, thus motivating the present research and leading to the following objectives of the thesis:

- a general way to synthesize the high-order linearizing PWM for balanced three-phase converters.

- a simple analog high-order linearizing PWM prototype circuit without multipliers/dividers.
- a circuit-oriented analysis technique for balanced three-phase converters.
- model and analysis of high-order linearizing PWM modulator.
- simulation and experimental verification.

This dissertation is organized as follows. Chapter 2 characterizes the low-frequency property of the PWM switch and reviews the switching-function averaging (SFA) technique. The derivation of the SFA state-space equations of a three-phase converter is presented. Components of balanced three-phase converters are modeled in the *ofb* coordinates, by which the time-variant three-phase converter can be graphically transformed into a time-invariant equivalent circuit for steady-state and dynamic analyses.

Chapter 3 reviews PWM techniques for dc and three-phase converters, in which large-signal linearization is emphasized. Two popular PWM techniques, sinusoidal PWM (SPWM) and space-vector modulation (SVM), are discussed in details in this chapter.

Chapter 4 identifies the nonlinear problem in three-phase converters. Two large-signal linearization techniques for three-phase PWM converters are proposed in this chapter. One technique uses several first-order linearizing PWM circuits to synthesize duty ratios for the switches in the converter individually. It involves multipliers/dividers to compute the inputs to the integrators. The other technique employs the proposed high-order LPWM circuit to

solve SFA equations. The inputs to the high-order LPWM circuit are linear functions of the control and input voltages. Therefore, no multipliers/dividers are required in the circuit, making analog implementation simple.

Chapter 5 focuses on the analysis of the LPWM-controlled converters. The large-signal and small-signal models of the LPWM are derived in this chapter. The time delay caused by sampling effects in the high-order LPWM is also investigated.

Chapter 6 concentrates on implementation and experimentation of the proposed analog high-order linearizing PWM. The experimental circuits and results are presented in this chapter.

Chapter 7 consists of the summary and conclusion of this dissertation.

CHAPTER 2
MODELING AND ANALYSIS OF THREE-PHASE CONVERTERS

This chapter presents the modeling and analysis techniques for three-phase PWM converters. These techniques are important for the synthesis and analysis of the linearizing pulsewidth modulation and three-phase PWM converters.

This chapter consists of six sections. The first section characterizes the low-frequency property of the PWM switch with switching-function averaging (SFA) technique. The derivation of the SFA state-space equations of a three-phase converter is presented. The second section transforms the SFA state-space equations into an equivalent circuit that is used for fast simulation. The third section reviews the *abc-ofb* transformation that is applied to the time-variant equivalent circuit to remove time dependency. The fourth section presents the graphical models for all components of the three-phase converter in the *ofb* coordinates. This section also demonstrates how to construct the time-invariant equivalent circuit of a three-phase converter in the *ofb* coordinates. The fifth section solves the *ofb* equivalent circuit graphically for the steady-state analysis. The sixth section derives the small-signal equivalent circuit by perturbing the control and input variables in the steady-state *ofb* equivalent

circuit. With the help of small-signal equivalent circuit, the control-to-output transfer function of the converter can be easily found graphically.

Although the boost inverter is used as an example to demonstrate the whole procedure, the analysis and modeling techniques in this chapter can be applied to any other three-phase PWM converter. To simplify explanation, it is assumed throughout the thesis that the components are ideal and the switches are lossless and four-quadrant.

2.1 Derivation of State-Space Equations of PWM Converters

2.1.1 Switching-Function Averaging Model of PWM Switch

To analyze the steady-state and dynamic performance of a PWM converter, which contains reactive components, the state-space equations must be presented. There are many approaches to derive the state-space equations for PWM converters, among which the state-space averaging technique [13, 14] is the most popular. This approach requires the identification of the switched networks and the derivation of the state-space equations for all switched networks that is easy to do in dc converters because of the small number of switched networks. However, a three-phase converter usually has a large number of switched topologies, and with the increase of phase numbers, the number of switched topologies will increase rapidly. For a given PWM method, the switched networks in one switching cycle can be different from those in another cycle. Moreover, different PWM schemes generate different switched

networks. Therefore, application of the state-space averaging technique to analyze three-phase converters is tedious.

Without probing into topological details, the switching-function averaging method [9, 15] treats the switch as a component in the same way as we treat other linear components by defining the PWM switch model. This allows derivation of state-space equations simply by inspection and application of definitions of circuit elements, Kirchhoff's laws, and other electrical principles. The switch model is derived by characterizing its low frequency property, as explained in this section.

The single-pole-multiple-throw (SPMT) switch shown in Figure 2-1 is one of the fundamental building elements in the PWM converters. The pole is usually connected to the inductor, and the throw is connected to either the voltage sources or the capacitors. The SPMT switch is reduced to a single-pole-double-throw (SPDT) switch in a dc converter; it may be SPDT or a single-pole-triple-throw (SPTT) switch in most three-phase converters.

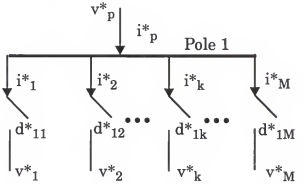


Figure 2-1 A single-pole-multiple-throw switch.

The operation of the throw k in Figure 2-1 is specified and modulated by the switching function d^*_{1k}, as shown in Figure 2-2, where the asterisk * denotes the instantaneous switching function. The function is one when the throw is closed and zero when the throw is open. A switching function defined this way can always be assigned to any throw in the converter without prior knowledge of modulation strategy or sequence of switched topologies. Therefore, this switch model allows derivation of state-space equations of a PWM converter without specifying modulation strategy. After the state-space equations are derived, they can be used for any PWM strategy to do a specific analysis [9].

In Figure 2-1, v^*_1-v^*_M are throw voltages, i^*_1-i^*_M are throw currents, i^*_p is the pole current, and v^*_p is the pole voltage. The asterisk * denotes the exact value. In switching functions shown in Figure 2-2 d_{11}-d_{1M} stand for duty ratios of switching functions. T_s is the switching period.

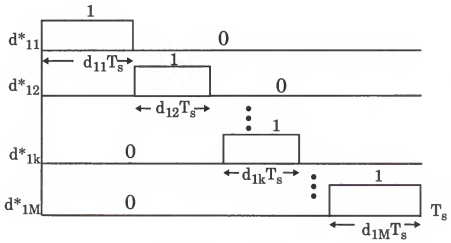


Figure 2-2 Switching functions of SPMT switches.

To avoid short circuit, no two throws turn on at the same time, and all switching functions must add up to one at any instant to avoid open circuit. In other words, one and only one of the switching functions of the SPMT switch is one at any instant. This can be expressed as follows:

$$\sum_{k=1}^{M} d^*_{1k} = 1 \tag{2.1}$$

It is obvious that there are only M-1 independent switching functions of the one-pole-M-throw switch.

At any moment, only one throw is connected to the pole. Therefore, the throw current equals pole current during its connection with the pole:

$$i^*_k = d^*_{1k} i^*_p \tag{2.2}$$

Over one switching cycle, the pole is connected to the throws one by one; thus, the pole voltage v^*_p is just a linear combination of the products of throw voltages and corresponding switching functions:

$$v^*_p = \sum_{k=1}^{M} d^*_{1k} v^*_k \tag{2.3}$$

The SPMT switches are switched at a high frequency. The voltages or currents connected with the pole and throws, either dc or sinusoidal ac, are varying slowly, relative to the switching frequency. Therefore, over one switching cycle, the terminal voltages and branch currents of the pole and throws can be assumed as constant. The duty ratio d_{1k} (without asterisk), which is the average of the switching function d^*_{1k} over the switching period T_s, is

modulated at a frequency sufficiently slower than the switching frequency. Therefore, the duty ratio is also assumed as constant over the switching cycle.

In the analysis and modeling of switched-mode converters, attention usually is restricted to low-frequency components of voltages and currents. The high-frequency components (also called ripples) are designed to be small and can be neglected due to the combination of fast switching and proper placement of filter corner frequencies. Therefore, the exact value with the asterisk in the previous switching-function equations can be, approximately, replaced by their low-frequency value for analysis and modeling of low-frequency components. This modeling technique is called switching-function averaging herein. The duty ratios in Equation (2.1) are then replaced by their averaged values:

$$\sum_{k=1}^{M} d_{1k} = 1 \tag{2.4}$$

The pole voltage and the throw currents in Equations (2.2) and (2.3) are replaced by their averaged values:

$$v_p = \sum_{k=1}^{M} d_{1k} v_k \tag{2.5}$$

$$i_k = d_k i_p \tag{2.6}$$

All values in Equations (2.4) - (2.6) vary slowly relative to the switching frequency; thus, they characterize the low-frequency properties of the SPMT switch shown in Figure 2-1. With these equations, the SPMT switches can be treated as components in the way we treat other components. The derivation

of state-space equations of a PWM converter becomes routine and can be done using state-space concept [16], definitions of circuit elements, Kirchhoff's laws, and other electrical principles.

2.1.2 Derivation of State-Space Equations

Since the SPMT switch in the converter has been modeled as a component by the switching-function averaging technique, there is no need to identify the switched topologies. State-space equations are derived simply by following the procedures described in ref 16. The only attention is to identify the SPMT switches in the converter. A three-phase boost inverter is used here to demonstrate how to identify the SPMT switches and how to derive state-space equations for PWM converters. Since the state-space equations of the switched-mode converter are derived by averaging the switching functions of the switch, they may be called switching-function-averaging state-space equations (SFA state-space equations) [9] in this thesis.

A three-phase boost inverter is illustrated in Figure 2-3. Since we know that the pole of the SPMT switch usually is connected with inductors and throw is connected with voltage sources or capacitors, it is easy to find that there are two single-pole-triple-throw (SPTT) switches in the three-phase boost inverter. The SPTT switch on the top consists of the switches S_{11}, S_{12}, and S_{13} and is characterized by d_{11}, d_{12}, and d_{13}. The SPTT switch on the bottom is grouped by S_{21}, S_{22}, and S_{23} and is characterized by d_{21}, d_{22}, and d_{23}. Duty ratios d_{11}- d_{23} correspond to the switching functions of switches S_{11}- S_{23},

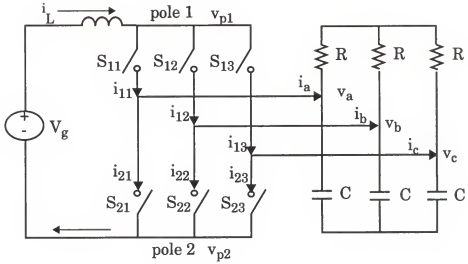


Figure 2-3 A three-phase boost inverter with two SPTT switches.

respectively, and they are modulated at a frequency sufficiently lower than the switching frequency.

The states of the inverter are inductor current i_L and capacitor voltages v_a, v_b, and v_c. The first pole voltage is v_{p1}, and the second pole voltage is v_{p2}. Based on the SFA model of the SPMT switch in Equations (2.4) - (2.6), v_{p1} and v_{p2} can be expressed as the linear combination of capacitor voltages and duty ratios of the switches:

$$v_{p1} = d_{11}v_a + d_{12}v_b + d_{13}v_c \tag{2.7}$$

$$v_{p2} = d_{21}v_a + d_{22}v_b + d_{23}v_c \tag{2.8}$$

The voltage across the inductor can be obtained by application of Kirchhoff's voltage law:

$$L\frac{di_L}{dt} = V_g - (v_{p1} - v_{p2}) \tag{2.9}$$

Combination of Equations (2.7) - (2.9) yields

$$L\frac{di_L}{dt} = V_g - d_a v_a - d_b v_b - d_c v_c \tag{2.10}$$

where d_a, d_b, and d_c are effective duty ratios:

$$d_a = d_{11} - d_{21} \qquad d_b = d_{12} - d_{22} \qquad d_c = d_{13} - d_{23} \tag{2.11}$$

Since the current through the switch is the product of the inductor current and the duty ratio of the switch according to Equations (2.4) - (2.6), the capacitor currents can be derived by applying Kirchhoff's current law as follows:

$$C\frac{dv_a}{dt} = (d_{11} - d_{21})i_L - \frac{2v_a - v_b - v_c}{3R} = d_a i_L - \frac{2v_a - v_b - v_c}{3R} \tag{2.12}$$

$$C\frac{dv_b}{dt} = (d_{12} - d_{22})i_L - \frac{2v_b - v_a - v_c}{3R} = d_b i_L - \frac{2v_b - v_a - v_c}{3R} \tag{2.13}$$

$$C\frac{dv_c}{dt} = (d_{13} - d_{23})i_L - \frac{2v_c - v_b - v_a}{3R} = d_c i_L - \frac{2v_c - v_b - v_a}{3R} \tag{2.14}$$

Equations (2.10) and (2.12) - (2.14) are called SFA state-space equations of the three-phase boost inverter. Although they are derived for the boost inverter, the switch model and the derivation procedure are general to other PWM converters.

The SFA state-space equations of the PWM converter are derived without knowledge of any PWM strategy and thus are general to any PWM modulation scheme: continuous sinusoidal PWM, space-vector modulating, and so forth. Once a specific PWM modulation technique is applied to the converter, the switching patterns and duty ratios in the SFA equations are known. For

the same PWM converter, a different PWM strategy leads to different coefficients in the SFA equations and state solutions.

The SFA state-space equations shown in Equations (2.10) and (2.12) - (2.14) are derived in the stationary reference frame or *abc* coordinates, in which all the state variables and coefficients in the equations are time-variant. Obviously, solving the time-variant state-space equations is very tedious and difficult. Therefore, they are transformed into the *ofb* coordinates to remove the time dependencies from the state-space matrices [15] by the *abc-ofb* transformation [17]. These coordinates consist of an *0*-sequence phasor, a *f*orward(-rotating) phasor, and a *b*ackward(-rotating) phasor. After the transformation, the SFA state-space equations become time-invariant, and the three-phase boost inverter can be analyzed by solving the state-space equations in the *ofb* coordinates. For a balanced three-phase system, the equations containing the *0*-sequence, forward, and backward phasors are completely decoupled. The steady-state backward phasors are directly related to the voltage and current phasors in the circuit. Unfortunately, the steady-state and dynamic analysis of converters [15], based on *ofb* state-space equations, contain intensive algebraic calculation and matrix manipulation. In addition, the equation-oriented model of the converter is not intuitive to computer simulation.

In contrast, circuit-oriented techniques [18, 19, 20, 21] are preferred for hand-analysis/calculation and computer simulation. Such circuit-oriented or "graphical" techniques not only produce the averaged equivalent circuit

of a PWM converter expeditiously, but also result in a model that is insightful and amenable to implementation in standard circuit simulators.

In the following section, the SFA state-space equations shown in Equation (2.10) and (2.12) - (2.14) are transformed into an equivalent circuit in the *abc* coordinates using the PWM Switch Model described in refs 18 and 19. This equivalent circuit is useful in fast simulation and prediction of various waveforms in the converter even though it is a time-variant circuit. Following this section, the thesis provides a technique that transforms a time-variant three-phase converter into a time-invariant equivalent circuit in the *ofb* coordinates. With the help of the *ofb* equivalent circuit, the steady-state and dynamic analysis of the three-phase converter becomes much easier.

2.2 Equivalent Circuit in the ABC Coordinates

According to the PWM-Switch-Model technique [18], the PWM switch can be modeled as a dc transformer that is a standard component in the simulator (such as Saber). The turns ratio is the duty ratio of the switching signal of the PWM switch. This technique is used in dc converters [18], but its idea can be extended to three-phase PWM converters or other PWM converters. Therefore, the SFA state-space equations of the PWM converter derived in the previous section can be transformed into an equivalent circuit using several dc transformers. This equivalent circuit is constructed by appropriate connections between the dc transformers and other components. The connections are

determined by the SFA state-space equations. The turns ratios of those dc transformers in the equivalent circuit are effective duty ratios in the SFA equations [22].

As an example, the three-phase boost inverter, as shown in Figure 2-3, is used to demonstrate the derivation of the equivalent circuit from the SFA state-space equations. The SFA equations of the three-phase boost inverter in Section 2.1.3 are organized and re-written as follows:

$$L\frac{di_L}{dt} = V_g - d_a V_a - d_b V_b - d_c V_c \tag{2.15}$$

$$C\frac{dv_a}{dt} = d_a i_L - \frac{2v_a - v_b - v_c}{3R} \tag{2.16}$$

$$C\frac{dv_b}{dt} = d_b i_L - \frac{2v_b - v_a - v_c}{3R} \tag{2.17}$$

$$C\frac{dv_c}{dt} = d_c i_L - \frac{2v_c - v_b - v_a}{3R} \tag{2.18}$$

A dc transformer is shown in Figure 2-4. Its turns ratio is determined by the duty ratio of the switching signal of the PWM switch. The duty ratios d_a, d_b, and d_c in the SFA equations shown in Equations (2.15) - (2.18) can be modeled by the dc transformer shown in Figure 2-4. The connection relationships between the transformers and other components in the boost inverter is defined by Equations (2.15) - (2.18). The resulting equivalent circuit of the three-phase inverter is shown in Figure 2-5. If the capacitor voltages v_a, v_b, and v_c are reflected from the output side to the input side, one can easily find that the inductor voltage of the equivalent circuit in Figure 2-5 is the same as

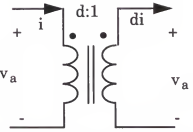


Figure 2-4 The dc transformer with the duty ratio of d.

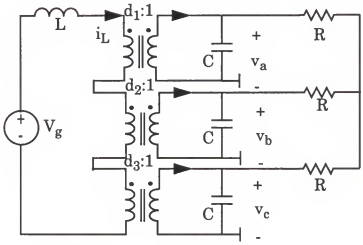


Figure 2-5 The equivalent circuit of the three-phase boost inverter in the *abc* coordinates.

that in Equation (2.15). The capacitor currents in the equivalent circuit also are found to be the same as those in Equations (2.16) - (2.18). Therefore, the equivalent circuit exactly represents the low-frequency properties of the three-phase boost inverter. Because there are no real switches in the equivalent circuit, the simulation of this circuit is expedited and memory space of the computer is also greatly saved. The simulation results of the equivalent circuit are the low-frequency components of the voltages and currents in the

inverter that are sufficient for us to predict various waveforms and design the inverter.

To appreciate how fast and accurate the equivalent circuit is, the circuit in Figure 2-5 is simulated in Saber. The simulation results are compared with the real-time simulation of the three-phase boost inverter. Supposing that the PWM method applied to the three-phase boost inverter is continuous SPWM, one choice for duty ratios is

$$\begin{bmatrix} d_{11} \\ d_{12} \\ d_{13} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} + \frac{D_m}{3}\sin(\theta_d) \\ \frac{1}{3} + \frac{D_m}{3}\sin\left(\theta_d - \frac{2\pi}{3}\right) \\ \frac{1}{3} + \frac{D_m}{3}\sin\left(\theta_d + \frac{2\pi}{3}\right) \end{bmatrix} \qquad \begin{bmatrix} d_{21} \\ d_{22} \\ d_{23} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} - \frac{D_m}{3}\sin(\theta_d) \\ \frac{1}{3} - \frac{D_m}{3}\sin\left(\theta_d - \frac{2\pi}{3}\right) \\ \frac{1}{3} - \frac{D_m}{3}\sin\left(\theta_d + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2.19}$$

The effective duty ratios are

$$\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} d_{11} - d_{22} \\ d_{12} - d_{22} \\ d_{13} - d_{23} \end{bmatrix} = \begin{bmatrix} \frac{2D_m}{3}\sin(\omega t) \\ \frac{2D_m}{3}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ \frac{2D_m}{3}\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2.20}$$

The simulated inverter has the following parameters: $D_m = 0.9$, $V_g = 200$ V, $\Omega = 2\pi(100$ Hz), R = 10 Ohm, C = 100 μF. The real-time simulation result is shown in Figure 2-6, and the time for 40 ms simulation is 30 seconds. The results of the simulation with the equivalent circuit is shown in Figure 2-7, and the time for 40 ms simulation is only 0.4 seconds.

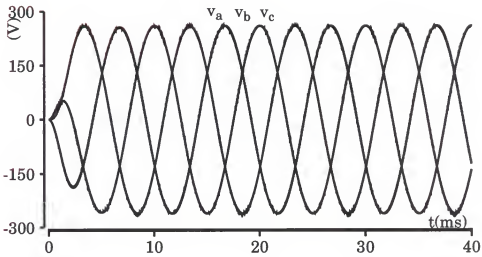


Figure 2-6 The real-time simulation of the three-phase boost inverter.

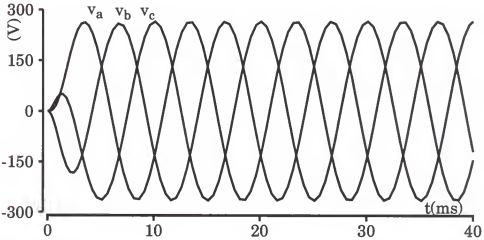


Figure 2-7 The simulation of the three-phase boost inverter with the equivalent circuit

Both simulations give the same output voltage:

$$V_a = 262\angle -32^O \tag{2.21}$$

The only difference between the two simulation results is that the real-time simulation contains the high-frequency ripple, but the equivalent circuit simulation has no ripple. The equivalent circuit produces exactly the low-frequency components of the output voltages. One interesting result obtained by both simulations is that the output voltage has a 32° phase shift from the control voltage, and the amplitude is also different from the value (222 V), predicted by the conversion ratio in Table 1.2 of Chapter 1, as shown in Figure 2-8. This interesting result can be easily predicted by the steady-state analysis of the *ofb* equivalent circuit of the three-phase boost inverter, which will be presented in the next section.

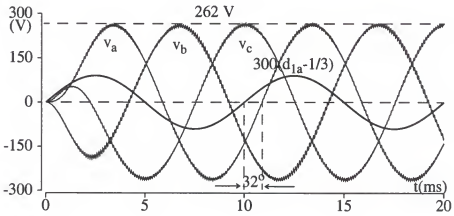


Figure 2-8 The real-time simulation results showing the phase shift and amplitude of the output voltages of the three-phase boost inverter.

The equivalent circuit in Figure 2-5 is derived in the *abc* coordinates that is a time-variant circuit. Although it is effective for the fast simulation,

the steady-state analysis, especially the dynamic analysis with the time-variant equivalent circuit, is tedious and difficult. Therefore, it must be transformed into the *ofb* coordinates or *odq* coordinates to remove the time dependency. Since *abc-odq* transformation leads to two coupled subcircuits [21], the resulting equivalent circuit is not convenient for analysis. The proposed time-invariant equivalent circuit in this thesis, however, is derived in the *ofb* coordinates, in which two subcircuits are completely decoupled, making the analysis much easier [22] and allowing one to write down answers by inspection.

2.3 ABC-OFB Transformation

The *abc-ofb* transformation matrix **T** transforms a time-varying vector $\mathbf{x}_{abc}$ in the stationary (*abc*) coordinates into a time-invariant complex vector $\mathbf{x}_{ofb}$ in the rotating (*ofb*) coordinates according to

$$\boldsymbol{x}_{abc} = \boldsymbol{T}\boldsymbol{x}_{ofb} \tag{2.22}$$

$$\boldsymbol{x}_{ofb} = \boldsymbol{T}^{-1}\boldsymbol{x}_{abc} \tag{2.23}$$

where, for a balanced three-phase system with positive phase sequence,

$$\boldsymbol{x}_{abc} = \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} x\cos(\theta_x) \\ x\cos(\theta_x - 2\pi/3) \\ x\cos(\theta_x + 2\pi/3) \end{bmatrix} \tag{2.24}$$

where

$$\theta_x(t) = \int_0^t \omega(\tau)d\tau - \phi_x \tag{2.25}$$

where ω is the instantaneous frequency;

$$\boldsymbol{T} = \frac{1}{\sqrt{3}}\begin{bmatrix} 1 & e^{-j\theta_T} & e^{j\theta_T} \\ 1 & e^{-j\left(\theta_T - \frac{2\pi}{3}\right)} & e^{j\left(\theta_T - \frac{2\pi}{3}\right)} \\ 1 & e^{-j\left(\theta_T + \frac{2\pi}{3}\right)} & e^{j\left(\theta_T + \frac{2\pi}{3}\right)} \end{bmatrix} \tag{2.26}$$

$$\boldsymbol{T}^{-1} = \frac{1}{\sqrt{3}}\begin{bmatrix} 1 & 1 & 1 \\ e^{j\theta_T} & e^{j\left(\theta_T - \frac{2\pi}{3}\right)} & e^{j\left(\theta_T + \frac{2\pi}{3}\right)} \\ e^{-j\theta_T} & e^{-j\left(\theta_T - \frac{2\pi}{3}\right)} & e^{-j\left(\theta_T + \frac{2\pi}{3}\right)} \end{bmatrix} \tag{2.27}$$

where

$$\theta_T(t) = \int_0^t \omega(\tau)d\tau - \phi_T \tag{2.28}$$

Note that $\mathbf{T}^{-1} = (\mathbf{T}^*)^T$ (the conjugate transpose matrix of **T**),

$$\boldsymbol{x}_{ofb} = \begin{bmatrix} x_o \\ x_f \\ x_{bw} \end{bmatrix} = \begin{bmatrix} 0 \\ \frac{\sqrt{3}}{2}x\, e^{j(\phi_x - \phi_T)} \\ \frac{\sqrt{3}}{2}x\, e^{-j(\phi_x - \phi_T)} \end{bmatrix} \tag{2.29}$$

where x_o is the zero-sequence component, x_f is the forward (rotating) phasor, and x_{bw} is the backward (rotating) phasor. Both ϕ_x and ϕ_T are the initial

phases. Note that x_f and x_{bw} are complex conjugates and constant (dc) under steady state.

2.4 Equivalent Circuit in the OFB Coordinates

2.4.1 Models of Three-Phase Components in the OFB Coordinates

A three-phase converter consists of resistors, inductors, capacitors, sources, and switches. Their models in the *ofb* coordinates are obtained by applying *abc-ofb* transformation and retaining Kirchhoff's voltage and current laws to their connectivity, that is, after transformation, circuit topology is the same as before. In the following analysis, **R** is the resistor matrix, **L** is the inductor matrix, **C** is the capacitor matrix, and **I** is the 3x3 identity matrix:

$$R = IR \qquad L = IL \qquad C = IC \tag{2.30}$$

Voltage sources. For the set of *abc* voltage sources in Figure 2-10(a), application of Equations (2.22) - (2.28) yields the set of *ofb* voltage sources in Figure 2-10(b). The *ofb* voltages/currents are found from the *abc* voltages/currents by Equation (2.29).

Resistors. For the set of *abc* resistors shown in Figure 2-10(c),

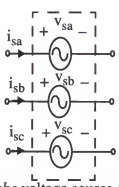
$$v_{Rabc} = Ri_{Rabc} \tag{2.31}$$

application of Equations (2.22) - (2.28) to (2.31) yields

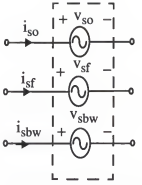
$$v_{Rofb} = Ri_{Rofb} \tag{2.32}$$

The *ofb* resistor set is thus as shown in Figure 2-10(d).

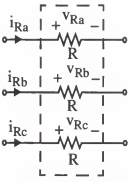
Inductors. For the set of *abc* inductors in Figure 2-10(e),



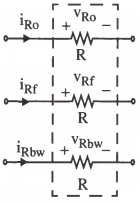
(a) *abc* voltage source set



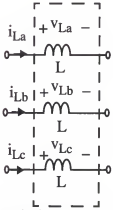
(b) *ofb* voltage source set



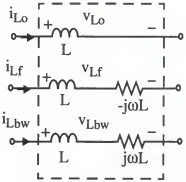
(c) *abc* resistor set



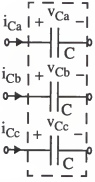
d) *ofb* resistor set



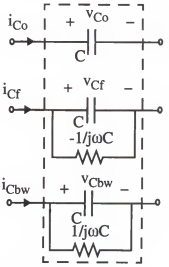
(e) *abc* inductor set



(f) *ofb* inductor set



(g) *abc* capacitor set



(h) *ofb* capacitor set

Figure 2-9 Graphical models of voltage sources, resistors, inductors, and capacitors in the *abc* coordinates and the *ofb* coordinates.

$$v_{Labc} = L\frac{di_{Labc}}{dt} \tag{2.33}$$

application of Equations (2.22) - (2.28) to (2.33) yields

$$\begin{aligned} v_{Lofb} &= T^{-1}L\frac{d(Ti_{\text{Lofb}})}{dt} = LT^{-1}\left(T\frac{di_{Lofb}}{dt} + \frac{dT}{dt}i_{Lofb}\right) \\ &= L\frac{di_{Lofb}}{dt} + \left(T^{-1}\frac{dT}{dt}L\right)i_{Lofb} \end{aligned} \tag{2.34}$$

where

$$T^{-1}\frac{dT}{dt}L = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -j\omega L & 0 \\ 0 & 0 & j\omega L \end{bmatrix} \tag{2.35}$$

The *ofb* inductor set is thus as shown in Figure 2-10(f). The *ofb* "inductor" is a real dynamic inductor L in series with an imaginary static resistor $\pm$ jωL.

Capacitors. The circuit models for the capacitors are the duals of those for the inductors and are shown in Figure 2-10(g) - 1(h).

Three-phase single-pole-double-throw (SPDT) switches. The SPDT switches shown in Figure 2-10(a) are commonly found, for example, in the buck inverter and boost rectifier [9]. Their low-frequency model in the *abc* coordinates is shown in Figure 2-10(b), where one choice for the duty ratios is

$$\begin{bmatrix} d_{a1} \\ d_{b1} \\ d_{c1} \end{bmatrix} = \begin{bmatrix} \frac{1}{2} + \frac{D_m}{2}\cos(\theta_d) \\ \frac{1}{2} + \frac{D_m}{2}\cos\left(\theta_d - \frac{2\pi}{3}\right) \\ \frac{1}{2} + \frac{D_m}{2}\cos\left(\theta_d + \frac{2\pi}{3}\right) \end{bmatrix} \qquad \begin{bmatrix} d_{a2} \\ d_{b2} \\ d_{c2} \end{bmatrix} = \begin{bmatrix} 1 - d_{a1} \\ 1 - d_{b1} \\ 1 - d_{c1} \end{bmatrix} \tag{2.36}$$

where

$$\theta_d(t) = \int_0^t \omega(\tau)\tau d\tau - \phi_d \tag{2.37}$$

The pole voltages and the throw currents can be expressed as

$$\begin{bmatrix} v_{pa} \\ v_{pb} \\ v_{pc} \end{bmatrix} = v_{pabc} = \begin{bmatrix} d_{a1} \\ d_{b1} \\ d_{c1} \end{bmatrix} v_{ts} = \mathbf{d}_{abc,1} v_{ts} \tag{2.38}$$

$$i_{ts} = \begin{bmatrix} d_{a1} & d_{b1} & d_{c1} \end{bmatrix} \begin{bmatrix} i_{pa} \\ i_{pb} \\ i_{pc} \end{bmatrix} = d^T_{abc,1} i_{pabc} \tag{2.39}$$

where $\mathbf{d}_{abc}{}^T$ is the transpose matrix of $\mathbf{d}_{abc}$. Note that the voltage reference node of the proceeding equations is assumed to be v_{t-}.

Application of Equations (2.22) - (2.28) to (2.38) and (2.39) yields

$$v_{pofb} = \mathbf{d}_{ofb,1} v_{ts} \qquad i_{ts} = (d^*_{ofb,1})^T i_{pofb} \tag{2.40}$$

where $(\mathbf{d}^*_{ofb,1})^T$ is the conjugate transpose of $\mathbf{d}_{ofb,1}$;

$$d_{ofb,1} = \left[\frac{\sqrt{3}}{2} \quad \frac{\sqrt{3}}{4} D_m e^{+j(\phi_d - \phi_T)} \quad \frac{\sqrt{3}}{4} D_m e^{-j(\phi_d - \phi_T)} \right]^T \tag{2.41}$$

The *ofb* model for the three-phase SPDT switches is, as shown in Figure 2-10(c). Note that the variables for the transformer in the *ofb* coordinates are generally complex. For a complex transformer, such as the one whose turns ratio is $1{:}\mathbf{d}_{bw1}$ in Figure 2-10(c), the transformation relationships are

$$v_{pbw} = d_{bw1} v_{ts} \qquad i_{ts-bw} = d^*_{bw1} i_{pbw} \tag{2.42}$$

where $\mathbf{d}^*_{bw1}$ is the conjugate of $\mathbf{d}_{bw1}$.

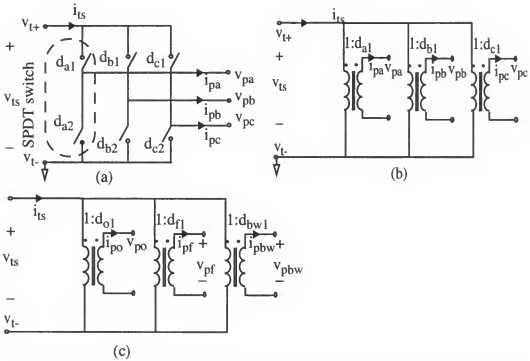


Figure 2-10 (a) Three-phase SPDT switches; (b) switch model in *abc* coordinates; (c) switch model in *ofb* coordinates.

Three-phase single-pole-triple-throw (SPTT) switches. The SPTT switches shown in Figure 2-11(a) are commonly found in, e.g., the boost inverter and buck rectifier [9]. Their low-frequency model in the *abc* coordinates is shown in Figure 2-11(b), where one choice for the duty ratios is

$$\begin{bmatrix} d_{1a} \\ d_{1b} \\ d_{1c} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} + \frac{D_m}{3}\cos(\theta_d) \\ \frac{1}{3} + \frac{D_m}{3}\cos\left(\theta_d - \frac{2\pi}{3}\right) \\ \frac{1}{3} + \frac{D_m}{3}\cos\left(\theta_d + \frac{2\pi}{3}\right) \end{bmatrix} \qquad \begin{bmatrix} d_{2a} \\ d_{2b} \\ d_{2c} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} - \frac{D_m}{3}\cos(\theta_d) \\ \frac{1}{3} - \frac{D_m}{3}\cos\left(\theta_d - \frac{2\pi}{3}\right) \\ \frac{1}{3} - \frac{D_m}{3}\cos\left(\theta_d + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2.43}$$

The effective duty ratios are

$$\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} d_{1a} - d_{2a} \\ d_{1b} - d_{2b} \\ d_{1c} - d_{2c} \end{bmatrix} = \begin{bmatrix} \frac{2D_m}{3}\cos(\theta_d) \\ \frac{2D_m}{3}\cos\left(\theta_d - \frac{2\pi}{3}\right) \\ \frac{2D_m}{3}\cos\left(\theta_d + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2.44}$$

The pole voltages and the throw currents can be expressed as

$$v_{ps} = \begin{bmatrix} d_a & d_b & d_c \end{bmatrix} \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} = d_{abc}^T v_{tabc} \tag{2.45}$$

$$\begin{bmatrix} i_{ta} \\ i_{tb} \\ i_{tc} \end{bmatrix} = i_{tabc} = \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} i_{ps} = d_{abc} i_{ps} \tag{2.46}$$

The voltage reference node of the proceeding equations is assumed to be the common node of the three-phase voltages. Application of Equations (2.22) - (2.28) to (2.45) and (2.46) yields

$$v_{ps} = (d_{ofb}^*)^T v_{tofb} \qquad\qquad i_{tofb} = d_{ofb} i_{ps} \tag{2.47}$$

where $(\mathbf{d}^*_{ofb})^T$ is the conjugate transpose matrix of $\mathbf{d}_{ofb}$;

$$d_{ofb} = \left[0 \;\; \frac{D_m}{\sqrt{3}} e^{+j(\phi_d - \phi_T)} \;\; \frac{D_m}{\sqrt{3}} e^{-j(\phi_d - \phi_T)} \right]^T \tag{2.48}$$

The *ofb* model for the three-phase SPTT switches is thus as shown in Figure 2-11(c). Before leaving this section, it is worth noting that, unlike the *d-q*

transformation, the *ofb* transformation results in decoupled zero-sequence, forward, and backward components subcircuits.

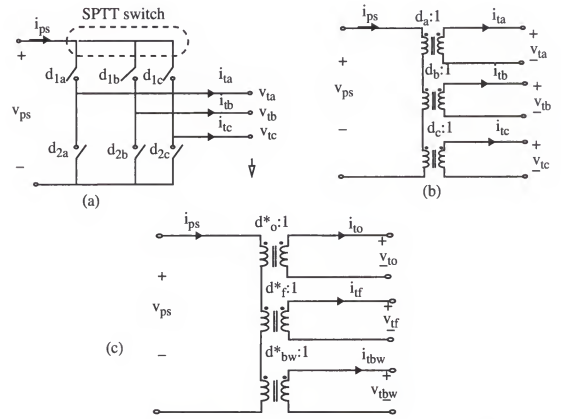


Figure 2-11 (a) Three-phase SPTT switches; (b) switch model in the *abc* coordinates; (c) switch model in the *ofb* coordinates.

2.4.2 Derivation of Equivalent Circuit in the OFB Coordinates

The equivalent circuit for a balanced three-phase PWM converter can be constructed graphically in the *ofb* coordinates just by replacing each set of three-phase switches by appropriately connected *ofb* transformers, and each set of three-phase components by the corresponding *ofb* component models. The resulting *ofb* equivalent circuit is time-invariant, in which the forward

component and backward component are totally decoupled. Therefore, the analysis of three-phase converters with the *ofb* equivalent circuit is easy.

To construct the *ofb* equivalent circuit, we need to identify dc and ac components in the *abc* coordinates. The ac components are replaced by their graphical models in the *ofb* coordinates, and dc components remain in the *ofb* equivalent circuit. As a result, the three-phase boost inverter is divided into five parts, as shown in Figure 2-12. Part one and part two are in the dc side of the inverter, including the dc voltage source and the inductor. In steady-state conditions, the inductor current is dc. Therefore, it is not necessary to transform the voltage source and inductor. Parts three, four and five are in the ac side of the inverter and include time-variant switches, capacitors, and resistors.

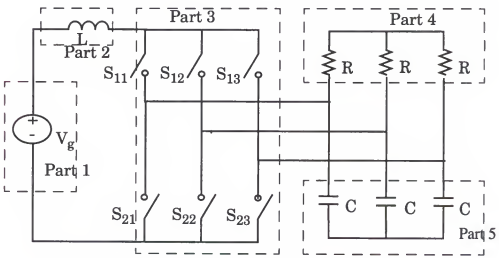


Figure 2-12 Partitioning the three-phase boost inverter.

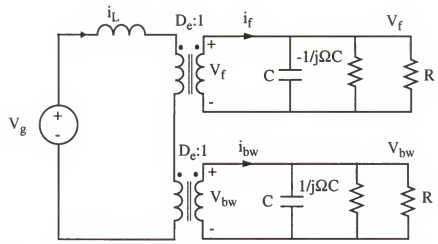


Figure 2-13 The equivalent circuit of the three-phase boost inverter in the *ofb* coordinates.

The ac components are transformed to their *ofb* models in the *ofb* equivalent circuit of the inverter. The resulting time-invariant equivalent circuit in *ofb* coordinates is shown in Figure 2-13. Since zero-sequence is zero in the balanced three-phase converter, the zero sequence circuit is excluded from Figure 2-13. The transformer turns ratios d_f and d_{bw} in the *ofb* circuit are time-invariant, and they have the same value when $\phi_d = \phi_T = 0$ in Equation (2.48) so that $D_f = D_{bw} = \frac{D_m}{\sqrt{3}}$, which is represented by D_e in Figure 2-13:

$$D_e = D_f = D_{bw} = \frac{D_m}{\sqrt{3}} \tag{2.49}$$

2.5 Graphical Steady-State Analysis

To analyze the three-phase boost inverter in the *ofb* coordinates under steady-state condition, replace all the inductors by short circuits and all the

capacitors by open circuits in the *ofb* equivalent circuit shown in Figure 2-13, the resulting steady-state equivalent circuit is shown in Figure 2-14.

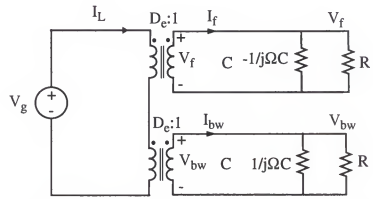


Figure 2-14 The steady-state equivalent circuit of the three-phase boost inverter in the *ofb* coordinate.

Reflecting the resistors (real and complex) in the secondary of the transformer to the primary, the circuit in Figure 2-14 becomes a simple circuit shown in Figure 2-15. Two conjugate resistors in Figure 2-15 form a voltage

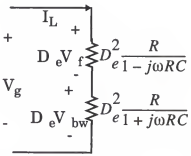


Figure 2-15 A simple circuit to solve the steady-state output voltage and inductor current.

divider; thus the backward voltage and inductor current can be obtained easily. The backward phasor is given by

$$V_{bw} = \frac{V_g}{2D_e}\left(1 - j\frac{\Omega}{\omega_p}\right) \tag{2.50}$$

that is the same as that derived from the equation-oriented method [9]. Substituting Equations (2.49) into (2.50) and applying Equation (2.29), the phasor of the output voltage v_a can be found as

$$V_a = \frac{V_g}{D_m}(1 - j\Omega RC) \tag{2.51}$$

The inductor current obtained from Figure 2-15 is a dc current, which is

$$I_L = \frac{3V_g}{2D_m^2 R}(1 + (\Omega RC)^2) \tag{2.52}$$

For D_m = 0.9, V_g = 200 V, Ω = 2π(100 Hz), R = 10 Ohm, C = 100 μF, $V_o = 262\angle -32^o$. This predicted output voltage agrees well with that obtained from real-time simulation, as is evident in Figure 2-8. Note that the reactive elements appears in the steady-state variables, introducing a right-half-plane zero. This right-half-plane zero causes some phase shift to the output voltage. In order to reduce the phase shift,

$$\Omega \ll \omega_p \tag{2.53}$$

2.6 Graphical Small-Signal Analysis

As shown in Figure 2-13, the two transformers in the *ofb* equivalent circuit are the same. They can be combined into one transformer with the turns ratio D_e, as shown in Figure 2-16. The transformer in the equivalent circuit

can be modeled as a voltage-control voltage source and a current-control current source, as shown in Figure 2-17(a).

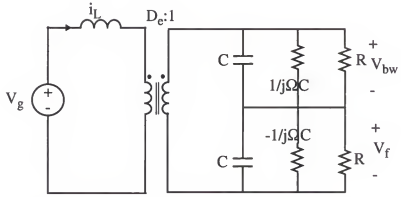


Figure 2-16 The equivalent circuit of the three-phase boost inverter in the *ofb* coordinates.

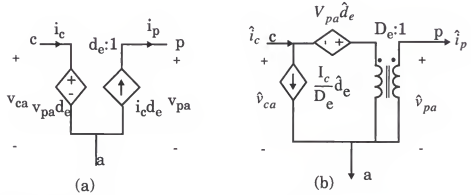


Figure 2-17 (a) The large-signal model of the dc transformer; (b) its small-signal model.

Application of small-signal perturbation to the capacitor voltage v_{pa}, the inductor current i_c, and the control variable d_e in the circuit yields

$$d_e = D_e + \hat{d}_e, \quad i_c = I_c + \hat{i}_c \ , \ v_{pa} = V_{pa} + \hat{v}_{pa} \tag{2.54}$$

where the caret implies small-signal perturbations. Neglect of the steady-state and second-order terms then leads to a small-signal equivalent circuit of the transformer, as shown in Figure 2-17(b). It consists of a dc transformer and two dependent sources that are controlled by the duty ratio. D_e, I_c, and V_{pa} in the capital letter are dc values derived from the steady-state analysis of the inverter. Replacing the transformer in Figure 2-16 by its small-signal circuit in Figure 2-17 yields the small-signal equivalent circuit of the inverter, as shown in Figure 2-18, where every variable is replaced by its small-signal value with the head "^".

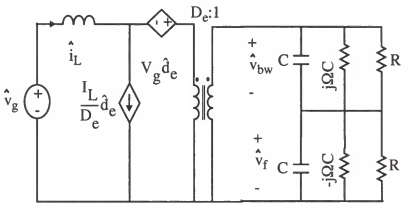


Figure 2-18 The small-signal equivalent circuit of the three-phase boost inverter.

Let $\hat{v}_g = 0$, the real part of control-to-output transfer function of the inverter can be solved from the small-signal circuit in Figure 2-18, which is given by

$$\frac{\hat{v}_r}{\hat{d}_e} = -\frac{V_g}{2D_e^2}\frac{\left(1-\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_{z1}}\right)}{D(s)} \tag{2.55}$$

the imaginary part is given by

$$\frac{\hat{v}_i}{\hat{d}_e} = -\frac{V_g}{2D_e^2\omega_p}\frac{\Omega\left(1-\frac{s}{\omega_z}\right)}{D(s)} \tag{2.56}$$

where

$$D(s) = 1+\left(RC+\frac{\Omega^2LC^2R}{2D_e^2}+\frac{L}{2D_e^2R}\right)s+\frac{LC}{D_e^2}s^2+\frac{LC^2R}{2D_e^2}s^3 \tag{2.57}$$

$$\omega_z = \frac{2D_e^2}{1+\left(\frac{\Omega}{\omega_p}\right)^2}\frac{R}{L} \qquad \omega_{z1} = \left[1+\left(\frac{\Omega}{\omega_p}\right)^2\right]\omega_p \tag{2.58}$$

$$\omega_p = \frac{1}{RC} \tag{2.59}$$

If the design allows

$$\left(\frac{\Omega}{\omega_o}\right)^2 \ll 1 \tag{2.60}$$

where the LC corner is located at

$$\omega_o = \sqrt{2}\frac{D_e}{\sqrt{LC}} \tag{2.61}$$

it suffices to approximate the poles by

$$D(s) \cong \left(1+\frac{s}{\omega_p}\right)\left(1+\frac{1}{Q}\frac{s}{\omega_o}+\left(\frac{s}{\omega_o}\right)^2\right) \tag{2.62}$$

where

$$Q = \frac{2D_e^2R}{\omega_oL} \tag{2.63}$$

From Equation (2.62), the poles of the three-phase boost inverter consist of a real pole and complex poles. Like the dc boost converter, the bandwidth is affected by the duty ratio D_e.

The control-to-output transfer function of the inverter can be found from Equations (2.55) and (2.56), which is given by

$$G(s) = \frac{\hat{v}_{om}}{\hat{d}_e} = -\frac{V_g}{2D_e^2}\sqrt{1+\left(\frac{\Omega}{\omega_p}\right)^2}\frac{\left(1-\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_{z1}}\right)}{D(s)} \tag{2.64}$$

Letting $\hat{d}_e = 0$, the input-to-backward phasor transfer function of the inverter can be found in the circuit in Figure 2-18, which is given by

$$\frac{\hat{v}_{bw}}{\hat{v}_g} = \frac{1}{2D_e}\frac{\left[1+\frac{s}{\omega_p}-j\frac{\Omega}{\omega_p}\right]}{D(s)} \tag{2.65}$$

The audiosusceptibility, that is, the input-to-output transfer function, is solved from Equation (2.65)

$$H(s) = \frac{\hat{v}_{om}}{\hat{v}_g} = \frac{1}{2D_e}\sqrt{1+\left(\frac{\Omega}{\omega_p}\right)^2}\frac{\left(1+\frac{s}{\omega_{z1}}\right)}{D(s)} \tag{2.66}$$

The transfer functions graphically derived from the small-signal equivalent circuit in Figure 2-18 completely agree with those derived by the equation-oriented method [9]. However, the graphical derivation is much simpler than the manipulation of state-space equations.

In conclusion, among existing modeling techniques, the switching-function averaging is the easiest technique to model three-phase converters. The equivalent circuit of the converter in the *abc* coordinates constructed from the

SFA state-space equations expedites the simulation. The equivalent circuit of the three-phase converters in the *ofb* coordinates is constructed graphically by replacing sets of three-phase components with appropriately connected *ofb* components. With the help of the *ofb* equivalent circuit, the steady-state and small-signal analyses of the three-phase converters can be worked out graphically, which is proven to be easier than the equation-oriented method.

CHAPTER 3
REVIEW OF PULSEWIDTH MODULATION

This chapter reviews the existing pulsewidth modulation (PWM) techniques for both dc converters and three-phase converters, in which large-signal linearization is emphasized. Two popular PWM methods for three-phase converters, continuous sinusoidal PWM (SPWM) and space-vector modulation (SVM), are discussed in detail.

3.1 Pulsewidth Modulation for DC Converters

The conventional PWM with a constant-slope carrier is the most popular in dc or single-phase converters, but it gives rise to undesirable nonlinear relationship between the output and control voltage in some topologies. Some linearizing PWM techniques (LPWM) have been proposed for linearization of dc or single-phase converters [10, 23-34]. In these PWM techniques, the slope of the carrier signal is not constant. Thus, the duty ratio generated from the LPWM is a nonlinear function of the input and control voltages that may cancel out the nonlinear control-to-output relationship of the converter and make the output voltage to track the control signal linearly.

3.1.1 One-Cycle Control

The one-cycle control [10, 23-28] has been widely used in various dc or single-phase PWM converters. When the one-cycle control was proposed in ref 10, the aim was to make the output voltage of the dc buck converter and Cuk converter follow the control voltage tightly without being disturbed by input voltage. It was subsequently proven that this control method can be easily used in other topologies, controls, and applications [23] - [28]. For instance, it can make the input current track the sinusoidal input voltage, allowing unit power factor to be obtained [25]. The basic concept of the one-cycle control is to force the average of the switched-variable, such as the diode voltage in the buck converter, to be proportional to the control variable in each switching cycle. Therefore, a one-cycle controller can make the output voltage proportional to the control voltage, that is, transform a switching power converter into a linear power amplifier in a large-signal sense. The one-cycle controller developed in ref 24 is a generalized circuit that can be used by any dc or single-phase PWM converter. In addition to the large-signal linearization of PWM converters, the one-cycle controller has some advantages over the conventional PWM techniques, such as the switching loss compensation, good line voltage regulation, and stable and simple control circuits.

3.1.2 Feed-Forward Pulsewidth Modulation

The feed-forward control is mostly used in the linear buck converter or buck-derived converters to reduce source disturbance on the output voltage,

where the slope of the ramp signal in the modulator varies with the input voltage. Its application in the nonlinear PWM converters is published in ref 12, in which good line voltage regulation is obtained for linear and nonlinear converters. However, the control-to-output gain is zero for the boost converter and nonlinear for "quadratic" converters [11].

The feed-forward control is adapted to a pulsewidth modulation [11]; it is called feed-forward PWM (FF-PWM). With the FF-PWM, any linear or nonlinear PWM converter can be linearized. The steady-state control-to-output relationship of the converter becomes linear regardless of operating conditions. The FF-PWM not only implements large-signal linearization of PWM converters, but also reduces the source disturbance on the output voltage of the converter. The FF-PWM has no stability problems and no effects on converter output impedance. If tight output voltage regulation is required, a small-signal voltage feedback can be used with less difficulty and with improved response compared with the conventional PWM modulation. Although the technique in ref [11] does not provide a general modulator circuit as the one-cycle controller, it provides us with a general way to synthesize the large-signal linearizing PWM circuit.

3.1.3 Peak-Current Mode Control

The peak-current mode control is widely used in dc or single-phase converters [35-37], in which the peak inductor current always equals the reference current, regardless of all other operating conditions. This control method

may be considered as a large-signal linearizing PWM in terms of linearization of the inductor current, such as the input current of the ac-dc converter. The output voltage, however, is still controlled by a nonlinear control-to-output relationship. Therefore, this control method needs an extra voltage feedback loop to linearize the output voltage and keep it stable. The current mode control has inherent advantages, such as fast dynamic response, automatic current protection, and so forth.

It is important to note that the carrier signals used in the above PWM methods are not constant, but they vary with the control signal from one switching cycle to another. They are herein called the PWM with a varying-slope carrier. The duty ratio generated from them is a nonlinear function of the control signal. This is different from the conventional PWM with a constant slope carrier. It is also worth noting that the slope of the carrier signal of PWM with varying-slope carrier is constant, that is, a straight line even though the slope rate changes from one switching cycle to another. The carrier used in refs 31 - 33, however, is nonlinear, which could be the exponential function.

The LPWM modulators previously discussed are general PWM methods suitable for all dc or single-phase PWM converter topologies, including linear and nonlinear converters. The LPWM circuits can be implemented by simple analog circuits, usually integrators and comparators. Although the PWM methods [38-41] are also able to implement large-signal linearization of the

PWM converters, they involve more sophisticated analog circuits, such as multipliers/dividers.

3.2 Pulsewidth Modulation for Three-Phase Converters

Three-phase PWM converters are employed in many areas of today's power industries, including active filtering [2], UPS [3], VAR compensation [4], power generation [5], motor drives [6, 7]. Compared with dc PWM converters, three-phase converters face more requirements, such as harmonics, balance/unbalance systems, and so forth. Moreover, they need more sophisticated control and drive circuits. Undoubtedly, linearization in PWM modulation will bring benefits, such as easier control, lower harmonic distortion, and source-disturbance rejection, to the three-phase PWM converters and help achieving the stringent application requirements.

Many PWM schemes for three-phase PWM converters have been published and applied in various power applications [42-58]. They can be classified into seven categories: sinusoidal, space-vector modulation, selective-harmonic-elimination, optimal, current control, direct amplitude control, and sigma-delta modulation.

3.2.1 Sinusoidal PWM

Sinusoidal PWM technique (SPWM) [42] is based on the principle of comparing a triangular carrier signal with a sinusoidal reference. The implementation of the technique with analog circuits is simple and can produce

very good sinusoidal waveforms. In recent years, much effort has been made toward digitization of the SPWM [43-46]. Online computation of instants of intersection of the triangular carrier and sinusoidal reference waveforms is not possible because no closed-form solution is available for intersection instants. Therefore, the reference sinusoidal waveforms have been replaced by trapezoidal [43], stepped [44], or triangular waveforms [45]. The carrier-based SPWM technique has disadvantages, such as attenuation of the fundamental component and large switching losses. Most of all, the slope of the high-frequency carrier in the PWM is constant and the duty ratios are linear functions of the reference signals. Therefore, the SPWM is unable to implement linearization of nonlinear PWM converters.

3.2.2 Space-Vector Modulation

Space-vector modulation [49] (SVM) can utilize most of the power source and reduce switching losses, which makes it the most popular PWM technique in three-phase converters. The SVM technique generates PWM signals by averaging the three switching-state vectors to equal the reference vector over each switching cycle. Since the SVM involves a significant amount of computation to determine the commutation instants of the switches, it is usually implemented by digital signal processor (DSP) or microprocessor [50]. The clock speed of the DSP or microprocessors, however, could impede the progress of PWM toward higher frequency. Analog implementation is an alternative to DSP for high-speed SVM. As with sinusoidal pulsewidth modulation, the SVM

can be implemented by comparing a six-step control signal, generated from the reference voltage, with a constant-slope carrier signal [1]. Such implementation, however, gives rise to nonlinear relationships between the control and output voltages, preventing the output voltages from tracking the control signals.

3.2.3 Optimal PWM

The optimal PWM technique [51] produces the switching pattern based on optimization of some performance criteria. The number and positions of the pulses or notches within each switching cycle are selected according to these criteria, which could be harmonic loss, torque pulsation, or load currents. They are precalculated and stored in memory for use in real time. Thus, computation power from a microprocessor is needed to synthesize the correct switching patterns.

3.2.4 Current-Controlled PWM

The current-controlled PWM technique [52] is intended to make the output current track the reference current. In this technique, the output currents with superimposing ripples are fed back and compared with hysteresis levels placed around the reference signal to determine the switching frequency. As the ripple is regulated within the hysteresis band, the average output follows the average reference. Three independent controllers are needed to control three phase legs separately in this scheme; each controller has its own

switching frequency related to its output. Although it has good dynamic performance, this technique suffers from low-frequency harmonics and high switching losses.

3.2.5 Selective-Harmonic-Elimination PWM

The selective-harmonic-elimination PWM technique [53] formulates a waveform that is chopped M times and possesses odd quarter-wave symmetry, and contains the information about where the pulse starts or ends. Therefore, any M harmonics can be nullified by solution of the corresponding M simultaneous transcendental equations, which need extensive numerical calculation. This technique is intended to attack the harmonics by suppressing an arbitrary number of them in the output spectrum.

3.2.6 Sigma-Delta Modulation

Sigma-delta modulation [54-57] consists of a hysteresis comparator and an integrator. The integrator estimates the reference voltage from the modulated PWM signal by low pass filter averaging. The estimated voltage is compared with the actual reference voltage through a hysteresis comparator to generate the error signal, which is quantized to form the PWM signal. Therefore, the output voltage, which is equivalent to the average of the modulated PWM signals, is able to follow the reference voltage within the hysteresis band. Sigma-delta modulation suffers from the problem of variable frequency and filter stability problems at high frequencies [56]. Although attempts have

been made to solve the variable frequency problem, they increase the complexity of the control circuit.

3.2.7 Direct Amplitude Control

The direct amplitude control [58] can make fundamental amplitude of the output voltage directly follow the reference voltage. Using Fourier analysis, the algorithm is to equalize the subamplitude of the output voltage with the subamplitude of the reference voltage for a complete fundamental cycle. This technique involves a significant computation; thus, it usually is implemented by DSP or microprocessor.

Among the above PWM techniques, the SPWM and SVM are the most popular in various three-phase converters. However, due to the constant-slope carrier, both PWM methods can produce a nonlinear relationship between the control and output voltages. This results in the output voltage failing to track the reference voltage linearly. Nevertheless, it can be shown that both SPWM and SVM can be developed into the linearizing PWM (LPWM) through the proposed large-signal linearization technique in this thesis. In the following sections, the conventional SPWM and SVM are discussed and synthesized, so that the proposed linearizing PWM can be better appreciated.

A three-phase boost inverter, shown in Figure 3-1, is used as an example to demonstrate how to synthesize the conventional SPWM and SVM.
The state-space equations of the inverter were given by Equations (2.15) - (2.18) in Chapter 2 and repeated here:

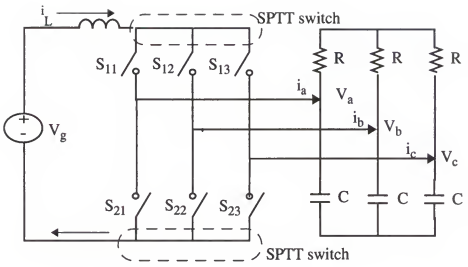


Figure 3-1 A three-phase boost inverter.

$$L\frac{di_L}{dt} = V_g - (d_{11} - d_{21})v_a - (d_{12} - d_{22})v_b - (d_{13} - d_{23})v_c \tag{3.1}$$

$$C\frac{dv_a}{dt} = (d_{11} - d_{21})i_L - \frac{2v_a - v_b - v_c}{3R} \tag{3.2}$$

$$C\frac{dv_b}{dt} = (d_{12} - d_{22})i_L - \frac{2v_b - v_a - v_c}{3R} \tag{3.3}$$

$$C\frac{dv_c}{dt} = (d_{13} - d_{23})i_L - \frac{2v_c - v_a - v_b}{3R} \tag{3.4}$$

In the above equations, v_a, v_b and v_c are balanced three-phase voltages. Their frequency and amplitude are known from the specifications:

$$v_a = V_m \sin(\omega t) \quad v_b = V_m \sin(\omega t - 120^o) \quad v_c = V_m \sin(\omega t + 120^o) \tag{3.5}$$

Duty ratios in the state-space equations d_{11} - d_{23} are unknown, which will be synthesized from Equations (3.1) - (3.4).

For a balanced three-phase system, Equation (3.2) can be expressed as

$$C\frac{dv_a}{dt} = (d_{11} - d_{21})i_L - \frac{v_a}{R} \tag{3.6}$$

Multiplying v_a on both sides yields

$$v_a C\frac{dv_a}{dt} = (d_{11} - d_{21})i_L v_a - \frac{v_a^2}{R} \tag{3.7}$$

The same procedure is applied to Equations (3.3) and (3.4) yields

$$v_b C\frac{dv_b}{dt} = (d_{12} - d_{22})i_L v_b - \frac{v_b^2}{R} \tag{3.8}$$

$$v_c C\frac{dv_c}{dt} = (d_{13} - d_{23})i_L v_c - \frac{v_c^2}{R} \tag{3.9}$$

Under steady state, the inductor current is assumed as dc; thus, di_L/dt in Equation (3.1) is zero. Substituting Equations (3.7) - (3.9) into (3.1) yields

$$V_g I_L = 3\frac{V_m^2}{2R} \tag{3.10}$$

$$I_L = 3\frac{V_m^2}{2RV_g} \tag{3.11}$$

It is obvious that Equation (3.10) is the conservation of power. The input inductor current is dc, the value is determined by Equation (3.11). Once I_L is obtained, duty ratios in Equations (3.7) - (3.9) can be solved from

$$(d_{11} - d_{21}) = \frac{C\frac{dv_a}{dt} + \frac{v_a}{R}}{I_L} = d_a \tag{3.12}$$

$$(d_{12} - d_{22}) = \frac{C\frac{dv_b}{dt} + \frac{v_b}{R}}{I_L} = d_b \tag{3.13}$$

$$(d_{13} - d_{23}) = \frac{C\frac{dv_c}{dt} + \frac{v_c}{R}}{I_L} = d_c \tag{3.14}$$

According to Equations (3.12) - (3.14), one can find that the effective duty ratios d_a, d_b and d_c are sinusoidal. Since the number of unknowns d_{11} -d_{23} in Equations (3.12) - (3.14) are more than the number of equations, we have more freedom to decide duty ratios, leading to many PWM techniques. A different modulation technique gives a different solution.

3.3 Synthesis of Continuous Sinusoidal Pulsewidth Modulation

In the continuous sinusoidal PWM (SPWM), the duty ratios d_{11} - d_{23} are continuous sinusoidal functions. In general, the duty ratio of each switch consists of a dc offset and a sinusoidal modulation. For a balanced three-phase converter, duty ratios d_{11} - d_{23} could be

$$\begin{bmatrix} d_{11} \\ d_{12} \\ d_{13} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} + \frac{D_m}{3}\sin(\omega t) \\ \frac{1}{3} + \frac{D_m}{3}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ \frac{1}{3} + \frac{D_m}{3}\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.15}$$

$$\begin{bmatrix} d_{21} \\ d_{22} \\ d_{23} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} - \frac{D_m}{3}\sin(\omega t) \\ \frac{1}{3} - \frac{D_m}{3}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ \frac{1}{3} - \frac{D_m}{3}\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.16}$$

where

$$D_m \leq 1 \tag{3.17}$$

The dc offset in Equations (3.15) and (3.16) is to keep the duty ratios positive. Equation (3.15) represents the sinusoidal modulation function for the top (single-pole-triple-throw) SPTT switches shown in Figure 3-1. Equation (3.16) represents the sinusoidal modulation function for the bottom SPTT switches shown in Figure 3-1. The amplitudes of the sinusoidal modulation function for the same switch group must be the same to constitute balanced three-phase sinusoids. The amplitudes and phases of sinusoidal modulation function for different switch groups could be different, as long as two switch groups are topologically independent. Note that the duty ratios in Equation (3.16) have the same amplitude and oppose phase from the duty ratios in Equation (3.15) that results in the optimal effective duty ratios:

$$\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} d_{11} - d_{22} \\ d_{12} - d_{22} \\ d_{13} - d_{23} \end{bmatrix} = \begin{bmatrix} \frac{2D_m}{3}\sin(\omega t) \\ \frac{2D_m}{3}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ \frac{2D_m}{3}\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.18}$$

that is related only to the continuous sinusoidal modulation techniques.

The amplitude D_m and the phase of duty ratio d_a in Equation (3.18) can be obtained from Equation (3.12), which is given by

$$|d_a| = D_m = \frac{3}{2}\frac{V_m\sqrt{1+(\omega RC)^2}}{RI_L} \tag{3.19}$$

$$\angle d_a = tan^{-1}(\omega RC) \tag{3.20}$$

where I_L is determined by Equation (3.11).

Combining Equations (3.11) and (3.19), one can find the amplitude of the output voltage is

$$V_m = \frac{V_g}{D_m}\sqrt{1+(\omega RC)^2} \tag{3.21}$$

3.4 Synthesis of Space-Vector Modulation

The balanced three-phase voltages v_a, v_b, and v_c are shown in Figure 3-2. In space-vector modulation (SVM), the phase voltages are divided into six segments, and each segment occupies 60°. In each segment, one SPTT switch in Figure 3-1 is permanently attached to one of the three capacitors as the other sweeps through all three. The position of the stationary switch, as well as the sweeping ones, are determined by six-step sequence.

In the first segment, 0°-60°, $v_b < v_a$ and $v_b < v_c$. Let $d_{22} = 1$, and $d_{21} = d_{23} = 0$, i. e., S_{22} is on, S_{21} and S_{23} are off all the time during this segment. The switches, S_{11}, S_{12}, and S_{13}, are switched at high switching frequency. The corresponding duty ratios, d_{11}, d_{13}, and d_{12}, are determined by Equations (3.12) - (3.14), respectively. Taking advantage of $d_{22} = 1$ and $d_{21} = d_{23} = 0$, then Equations (3.12) - (3.14) become

$$d_{11} = \frac{C\frac{dv_a}{dt} + \frac{v_a}{R}}{I_L} = d_a \tag{3.22}$$

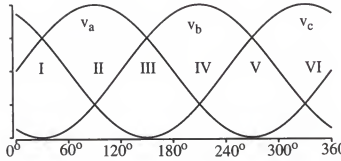


Figure 3-2 The balanced three-phase voltages.

$$(d_{12}-1) = \frac{C\dfrac{dv_b}{dt}+\dfrac{v_b}{R}}{I_L} = d_b \tag{3.23}$$

$$d_{13} = \frac{C\dfrac{dv_c}{dt}+\dfrac{v_c}{R}}{I_L} = d_c \tag{3.24}$$

From Equations (3.22) and (3.24), it can be found that d_{11} and d_{13} are sinusoids, and d_{12} is the sinusoid with the dc offset. In summary, during 0° - 60°, the duty ratios for the switches are

$$d_{11} = D_m \sin(\omega t) \tag{3.25}$$

$$d_{13} = D_m \sin\left(\omega t + \frac{2\pi}{3}\right) \tag{3.26}$$

$$d_{12} = 1 + D_m \sin\left(\omega t - \frac{2\pi}{3}\right) \tag{3.27}$$

$$d_{21} = d_{23} = 0 \qquad d_{22} = 1 \tag{3.28}$$

where the amplitude D_m and the phase of the duty ratio d_{11} can be obtained from Equation (3.22) as the following:

$$|d_{11}| = D_m = \frac{V_m\sqrt{1+(\omega RC)^2}}{RI_L} \tag{3.29}$$

$$\angle d_a = tg^{-1}(\omega RC) \tag{3.30}$$

The effective duty ratios are

$$\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} d_{11}-d_{22} \\ d_{12}-d_{22} \\ d_{13}-d_{23} \end{bmatrix} = \begin{bmatrix} D_m \sin(\omega t) \\ D_m \sin\left(\omega t - \frac{2\pi}{3}\right) \\ D_m \sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.31}$$

Combination of Equations (3.11) and (3.29) yields

$$V_m = \frac{2}{3}\frac{V_g}{D_m}\sqrt{1+(\omega RC)^2} \tag{3.32}$$

In fact, the three-phase boost inverter works like a dc boost converter. When S_{12} is on, the inductor gets energy from the source. When either S_{11} or S_{13} is on, the inductor transfers the energy to the load. Since only one SPTT is switched at high frequency and the other is switched at low frequency, the SVM has less switching loss than continuous SPWM.

The duty ratios d_{11} - d_{23} for the six segments are listed in Table 3.1, and their waveforms over one period are shown in Figure 3-3. It is obvious that the duty ratio functions in the SVM are piecewise sinusoidal and have six-step symmetry.

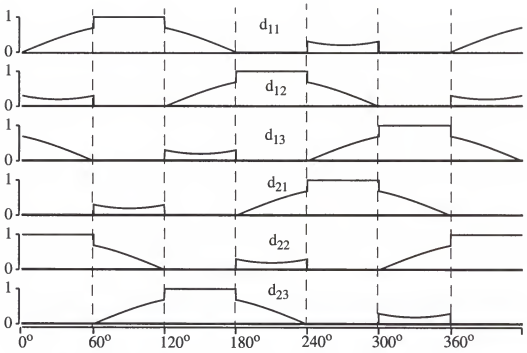


Figure 3-3 Duty ratios for space-vector modulation.

Table 3.1 Duty ratios for the three-phase boost Inverter with the SVM.

STEP	d_{11}	d_{12}	d_{13}	d_{21}	d_{22}	d_{23}
1	$D_m \sin(\omega t)$	$1 + D_m \sin\left(\omega t - \frac{2\pi}{3}\right)$	$D_m \sin\left(\omega t + \frac{2\pi}{3}\right)$	0	1	0
2	1	0	0	$1 - D_m \sin(\omega t)$	$-D_m \sin\left(\omega t - \frac{2\pi}{3}\right)$	$-D_m \sin\left(\omega t + \frac{2\pi}{3}\right)$
3	$D_m \sin(\omega t)$	$D_m \sin\left(\omega t - \frac{2\pi}{3}\right)$	$1 + D_m \sin\left(\omega t + \frac{2\pi}{3}\right)$	0	0	1
4	0	1	0	$-D_m \sin(\omega t)$	$1 - D_m \sin\left(\omega t - \frac{2\pi}{3}\right)$	$-D_m \sin\left(\omega t + \frac{2\pi}{3}\right)$
5	$1 + D_m \sin(\omega t)$	$D_m \sin\left(\omega t - \frac{2\pi}{3}\right)$	$D_m \sin\left(\omega t + \frac{2\pi}{3}\right)$	1	0	0
6	1	0	0	$-D_m \sin(\omega t)$	$-D_m \sin\left(\omega t - \frac{2\pi}{3}\right)$	$1 - D_m \sin\left(\omega t + \frac{2\pi}{3}\right)$

CHAPTER 4
HIGH-ORDER LINEARIZING PULSEWIDTH MODULATOR

This chapter investigates the feasibility of large-signal linearization of three-phase PWM converters by analog linearizing pulsewidth modulator (LPWM). The study shows that three-phase PWM converters have nonlinear relationships between the control and output voltages when they are controlled by the conventional analog SPWM or SVM modulators. Some sophisticated analog circuits may employ analog multipliers/dividers to compute the switching instants for three-phase converters to implement linearization. However, the complexity of the resulting circuitry makes them impractical. The first-order linearizing PWM circuit uses integrators to compute commutation instants to linearize control-to-output relationship in dc or single-phase converters. They can also be used to control three-phase converters, but, as indicated in this chapter, the inputs to the integrators are nonlinear function of control voltages, resulting in use of analog multipliers/dividers.

A high-order linearizing PWM modulator is developed in this chapter. It is able to make output voltages of three-phase PWM converters track control signals linearly even in the nonlinear topologies. Instead of multipliers/dividers, the high-order linearizing PWM uses only integrators with the reset, and sample/hold to compute the switching instants for the switches. The

inputs to the integrators are just linear functions of the control and state variables.

In the first section of this chapter, the first-order LPWM is reviewed, which is helpful to understand the concept of large-signal linearization and analog implementation of the LPWM. The nonlinear problem, caused by the conventional PWM modulator in three-phase PWM converters, is identified in the second section. A general way to linearize PWM converters is discussed in the third section. Implementation of the LPWM modulator by first-order LPWM circuits for a three-phase inverter is given in the fourth section. The fifth section presents the high-order LPWM that linearizes three-phase converters with simple analog circuits. The techniques to synthesize a high-order LPWM and eliminate multipliers/dividers in the LPWM circuit of three-phase converters is discussed. An analog implementation of the high-order LPWM for a three-phase converter is derived and simulated.

4.1 First-Order Linearizing Pulsewidth Modulator

The carrier signal in the conventional PWM modulator has the fixed frequency and constant slope. The duty ratio of switching signals generated by the conventional PWM is directly proportional to the control signal. The carrier signal in the linearizing PWM (LPWM) has the fixed frequency, but varying slope. The duty ratio generated from the LPWM is a nonlinear function of the control signal and input voltage.

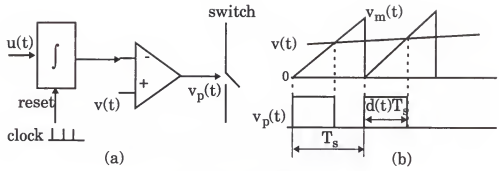


Figure 4-1 (a) A first-order linearizing PWM; (b) its operation waveform.

The first-order LPWM modulator usually consists of a resetable integrator and a comparator, as shown in Figure 4-1(a). Its operation waveform is illustrated in Figure 4-1(b). When the clock signal comes, the output signal v_p of the comparator becomes high, turning on the switch in the converter. At the same time, the integrator starts to integrate the input signal u(t). When the integrator output reaches comparator input v(t), the output pulse drops to low and turns the switch off, as shown in Figure 4-1(b).

It is supposed that the clock is sufficiently fast so that the function u(t) and v(t) can be assumed as constant over each switching cycle. Therefore, the amplitude of the ramp generated by the integrator is

$$v_m = \frac{1}{T_s}\int_0^{T_s} u(t)dt \approx u(t) \tag{4.1}$$

The slope of the carrier ramp varies with u(t), which is

$$Slope = \frac{u(t)}{T_s} \tag{4.2}$$

The average value of u(t) over one switching cycle is given by

$$\frac{1}{T_s}\int_0^{d(t)T_s} u(t)dt \approx u(t)d(t) \tag{4.3}$$

which equals the comparator input v(t):

$$u(t)d(t) = v(t) \tag{4.4}$$

In most of dc converters, the relationship between the output voltage and the duty ratio can be expressed in the form of Equation (4.4). For example, the average output voltage V_o of a dc-dc boost converter is the function of duty ratio and the input voltage:

$$V_o = \frac{V_g}{1-D} \tag{4.5}$$

Transformed into the form of Equation (4.4), then (4.5) becomes

$$V_o D = V_o - V_g \tag{4.6}$$

If the boost converter is controlled by the first-order LPWM shown in Figure 4-1(a), and let $v(t) = V_c - V_g$ and $u(t) = V_c$, the duty ratio can be given as

$$D = \frac{V_c - V_g}{V_c} \tag{4.7}$$

Substitution of Equation (4.7) to (4.5) yields

$$V_o = V_c \tag{4.8}$$

Note that the average output voltage V_o of a nonlinear boost converter can track the control voltage linearly, as indicated in Equation (4.8).

Some dc converters have quadratic duty ratios in the control-to-output relationship [11] [24]. They can still be linearized by the LPWM, as shown in Figure 4-1, but adding one more integrator and gain block to it. This is because

$$uD^2 = u\left(\frac{t_{on}}{T_s}\right)^2 \approx \frac{2}{T_s}\int_0^{DT_s}\frac{1}{T_s}\left(\int_0^{DT_s} u(\tau)d\tau\right)dt \tag{4.9}$$

4.2 Nonlinear Problem in Three-Phase Converters

The nonlinear relationship between the output and control voltages exists in most three-phase PWM converters that are controlled by conventional PWM modulations, such as sinusoidal PWM (SPWM) and space-vector modulation (SVM). The high-frequency carrier signal in the conventional SPWM and SVM has a constant slope. The duty ratios of switching signals generated by these PWMs are proportional to the control voltages, which are not able to cancel the nonlinear duty-ratio-to-output relationship of the converters. As a result, output voltages are not able to track the control signals linearly. In the balanced three-phase converters, the output waveform is sinusoidal, not affected by this nonlinear control-to-output relationship. The amplitude, however, is affected by the nonlinear control-to-output relationship.

As an example, a balanced three-phase boost inverter, as shown in Figure 4-2, is used to demonstrate the nonlinear problem in three-phase converters. It is controlled by the conventional SPWM. The input voltage V_g is dc, the

three-phase output voltages v_a, v_b, and v_c are purely sinusoidal. The control voltages v_{cntl-a} and v_{cntl-b} into the SPWM are sinusoidal waveforms with the amplitude D_m:

$$v_{cntl-a} = \frac{1}{3} + \frac{D_m}{3}\sin(\omega t) \tag{4.10}$$

$$v_{cntl-b} = \frac{1}{3} + \frac{D_m}{3}\sin(\omega t - 120^o) \tag{4.11}$$

The dc offset in the control voltages is needed to guarantee the duty ratio positive.

The control voltages are compared with the constant-slope carrier in the SPWM. The duty ratios of the resulting PWM signals are proportional to

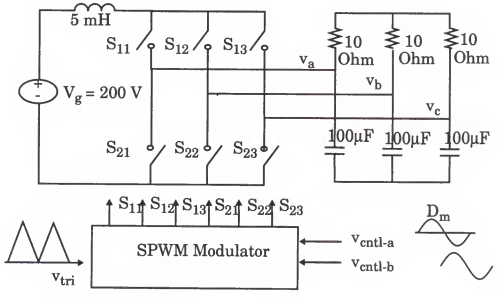


Figure 4-2 The three-phase boost inverter controlled by the conventional SPWM modulator.

the control voltages in Equations (4.10) and (4.11). According to the theory of the balanced three-phase inverter in Chapter 2 and the SPWM in Chapter 3, the output voltages remain balanced sinusoidal waveforms, but their amplitude becomes inversely proportional to the amplitude of the control voltage:

$$V_m = \frac{V_g}{D_m}\sqrt{1+(\omega RC)^2} \tag{4.12}$$

Therefore, the output voltages are not able to track the control voltage linearly in the boost converter. This nonlinear relationship is verified by the simulation results. The amplitudes of the output voltages for different control voltages for shown in Figure 4-3.

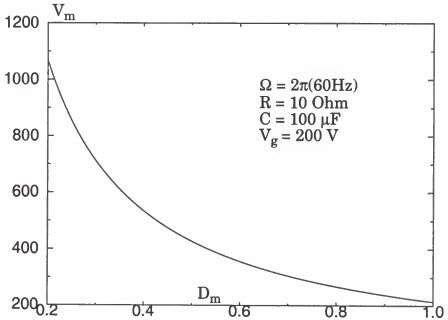


Figure 4-3 The amplitude of the output voltages versus the amplitude of control voltages for the ideal case.

4.3 Large-Signal Linearization of PWM Converters

A typical PWM converter controlled by the LPWM is shown in Figure 4-4. The PWM converter could have single or multiple input/output variables. The variables at the input/output side could be dc or ac. For example, in three-phase inverters, the input is dc voltage and the output are three-phase voltages, in which the output voltages are controlled variables. In three-phase rectifiers, the inputs are three-phase voltages and the output is dc voltage, where both output dc voltage and the input currents are controlled variables. In order to simplify the explanation of large-signal linearization technique presented in this thesis, we consider only the output voltage $\mathbf{v_o}$ as the controlled variable. The objective is to make the output voltage $\mathbf{v_o}$ track the control voltage $\mathbf{v_c}$ linearly through the LPWM.

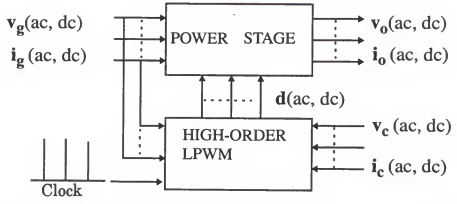


Figure 4-4 The converter controlled by the high-order LPWM.

In PWM converters, the output voltage, $\mathbf{v_o}$, is controlled by duty ratio **d**:

$$v_o = f(d, v_g) \tag{4.13}$$

which is the nonlinear function of the duty ratio in most of PWM converters. When it is controlled by the conventional PWM, the duty ratio is proportional to the control voltage.

$$d = v_c \tag{4.14}$$

The resulting output voltage will be the nonlinear function of the control voltage:

$$v_o = f(v_c, v_g) \tag{4.15}$$

However, the large-signal LPWM in Figure 4-4 is synthesized by (4.13). It is able to solve (4.13) and find duty ratio as the function of the output voltage and input voltage:

$$d = f^{-1}(v_o, v_g) \tag{4.16}$$

The output voltage thus equals the control voltage:

$$v_o = v_c \tag{4.17}$$

According to (4.17), the output voltage of the nonlinear PWM converter controlled by the LPWM is able to track the control voltage linearly. The nonlinear control-to-output relationship is completely eliminated without using any feedback loop.

In general, the task of the LPWM controller is to obtain the duty ratio by solving modulation Equation (4.16), which could be done either by digital signal processors (DSP) or by analog circuits. Even though only analog imple-

mentation of the LPWM is discussed in this thesis, it is intended to parallel the recent advances in analog first-order LPWM techniques for dc or single-phase converters [11, 24].

Analog implementation of the LPWM could be done by the conventional PWM and nonlinear modulation function in Equation (4.16). To synthesize the control voltage given by Equation (4.16), multipliers/dividers or other sophisticated circuits must be used. As a result, the complexity of the resulting circuitry makes them impractical.

To avoid complicated circuits such as multipliers/dividers, the integrator (with reset) are used by the first-order LPWM to solve modulation Equation (4.16) in dc or single-phase converters [11, 24], as shown in Section 4.1 of this chapter. The first-order LPWMs can be used for some three-phase converters, as long as the modulation equation does not have nonlinear terms of control signals [59, 60].

For most three-phase converters, a modulation equation (4.16) usually contains some nonlinear terms of control signals. The synthesis of the LPWM with first-order modulators, therefore, will involve multipliers/dividers. The high-order LPWM technique developed in this thesis is able to eliminate the nonlinear terms of control voltages in the modulation equation (4.16). The resulting circuitry, called high-order LPWM, contains integrators with reset and hold, and also comparators. The inputs to integrators are just linear functions of control voltages. Therefore, the high-high LPWM is simple and easy to use.

In the following sections, a general procedure is presented to use first-order LPWM circuits to synthesize the LPWM for three-phase converters. Although it may end up with using multipliers/dividers in the LPWM circuit, the synthesis procedure is still helpful to understand the linearization of three-phase converters and use first-order LPWM modulators in three-phase converters.

4.4 Linearization by First-Order LPWM

The first step to linearize three-phase converters by first-order LPWM circuits is to find the SFA equations of the converter. The derivation of the SFA equations of a PWM converter is discussed in Chapter 2. For a PWM converter with M independent switches, the duty ratios of the switching signals for these M switches are defined as:

$$d^T = [d_1, d_2, \ldots, d_M] \tag{4.18}$$

After solving SFA equations of the converter, each variable in Equation (4.18) can be expressed as a function of the output voltage $\mathbf{v_o}$ and input voltage $\mathbf{v_g}$:

$$d_1 = \frac{P_1(v_g, v_r)}{Q_1(v_g, v_r)} \tag{4.19}$$

$$d_M = \frac{P_M(v_g, v_r)}{Q_M(v_g, v_r)} \tag{4.20}$$

where the output voltage $\mathbf{v_o}$ is replaced by the reference voltage $\mathbf{v_r}$. For example, the duty ratios of the three-phase boost inverter shown in Figure 3-1 of Chapter 3, d_{11} - d_{13}, are functions of input voltage V_g and output voltages

determined by Equations (3.16), (3.19), and (3.20) in Chapter 3. When controlled by the duty ratios shown in Equations (4.19) - (4.20), the output voltage should equal to the reference voltage. It is worth noting that the duty ratios expressed by Equations (4.19) - (4.20) are only dependent on the reference voltage and input voltage, and they are not coupled with each other. Therefore, they can be synthesized individually by M first-order LPMW circuits.

To synthesize the duty ratios using the first-order LPWM circuits, transform (4.23) - (4.24) into the following forms:

$$Q_1(v_{in}, v_r)d_1 = P_1(v_{in}, v_r) \tag{4.21}$$

$$Q_M(v_{in}, v_r)d_M = P_M(v_{in}, v_r) \tag{4.22}$$

Assume that the duty ratios d_1 - d_M are uniquely determined by the input voltage and the reference voltages of the converter in each of the above equations. Additionally, it is assumed that the switching frequency is sufficiently high, and the input voltage and the reference voltage vary slowly, so that the input voltages and the reference voltages can be treated as constant during each switching cycle. This is true because the sinusoidal signal, which is needed to be synthesized in most power applications, is usually 60 Hz, but the switching frequency could be as high as several KHz to several hundred KHz. Various losses in the converter are neglected to simplify the analysis. These losses can be compensated by the feedback circuit in practice. With the above assumptions, (4.21) - (4.22) may be transformed into the integration forms:

$$\frac{1}{T_s}\int_0^{T_s d_1} Q_1(v_g, v_r)dt = P_1(v_g, v_r) \tag{4.23}$$

$$\frac{1}{T_s}\int_0^{T_s d_M} Q_M(v_g, v_r)dt = P_M(v_g, v_r) \tag{4.24}$$

Each of these integration equations can be implemented by a first-order LPWM circuit with a resetable integrator and one comparator, as shown in Figure 4-5. The operation waveform can be referred to Figure 4-1(b).

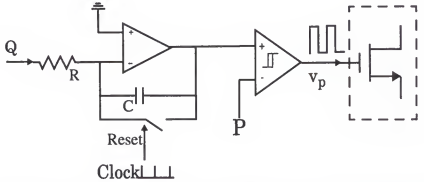


Figure 4-5 The first-order LPWM circuit to synthesize one of the duty ratios.

When the clock signal is coming, the Q function is integrated, and the output of the integrator is compared with the P function. During this time, the PWM signal v_p is high, turning on the switch in the converter. When the output of the integrator ramps up to the P function, the PWM signal v_p becomes low, turning off the switch. The resulting duty ratio of PWM signal v_p is

$$d_p = \frac{P(v_g, v_r)}{Q(v_g, v_r)} \tag{4.25}$$

The P function and Q function in the LPWM circuit are functions of the input and reference voltages, which can be synthesized from the input and reference voltages by operational circuits, such as adders/subtractors, and multipliers/dividers, as shown in Figure 4-6.

As an example, consider the large-signal linearization of a three-phase boost inverter, as shown in Figure 4-7. This converter consists of six switches

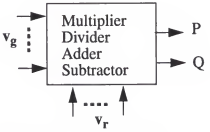


Figure 4-6 P function and Q function generator.

(two single-pole-triple-throw switches), but only four of these switches are independent. This is because

$$d_{11} + d_{12} + d_{13} = 1 \tag{4.26}$$

$$d_{21} + d_{22} + d_{23} = 1 \tag{4.27}$$

The sinusoidal PWM (SPWM) technique discussed in Chapter 3 is applied in the inverter. One of choices of duty ratios is

$$\begin{bmatrix} d_{11} \\ d_{12} \\ d_{13} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} + \frac{D_m}{3}\sin(\omega t) \\ \frac{1}{3} + \frac{D_m}{3}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ \frac{1}{3} + \frac{D_m}{3}\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{4.28}$$

$$\begin{bmatrix} d_{21} \\ d_{22} \\ d_{23} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} - \frac{D_m}{3}\sin(\omega t) \\ \frac{1}{3} - \frac{D_m}{3}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ \frac{1}{3} - \frac{D_m}{3}\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{4.29}$$

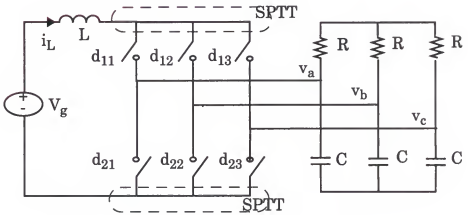


Figure 4-7 The three-phase boost inverter.

The SFA state-space equations derived from the three-phase inverter are

$$L\frac{di_L}{dt} = V_g - (d_{11} - d_{21})v_a - (d_{12} - d_{22})v_b - (d_{13} - d_{23})v_c \tag{4.30}$$

$$C\frac{dv_a}{dt} = (d_{11} - d_{21})i_L - \frac{2v_a - v_b - v_c}{3R} \tag{4.31}$$

$$C\frac{dv_b}{dt} = (d_{12} - d_{22})i_L - \frac{2v_b - v_a - v_c}{3R} \tag{4.32}$$

Under steady-state condition, Substitution of Equations (4.28) and (4.29) into (4.30) - (4.32) and application of a simple algebra manipulation, they yields

$$d_{11}v_b - d_{12}v_a = \frac{1}{3}(v_b - v_a) \tag{4.33}$$

$$d_{11}(v_a - v_c) + d_{12}(v_b - v_c) = \frac{V_g}{2} - v_c \tag{4.34}$$

From Equations (4.33) and (4.34), duty ratios d_{11} and d_{12} can be found as the nonlinear functions of the input and output voltages:

$$d_{11} = \frac{\frac{1}{3}(v_a^2 + v_b^2 + v_c^2) + \frac{V_g}{2}v_a}{v_a^2 + v_b^2 + v_c^2} \tag{4.35}$$

$$d_{12} = \frac{\frac{1}{3}(v_a^2 + v_b^2 + v_c^2) + \frac{V_g}{2}v_b}{v_a^2 + v_b^2 + v_c^2} \tag{4.36}$$

From Equations (4.28) and (4.29), we can find that

$$d_{21} = \frac{2}{3} - d_{11} \quad d_{22} = \frac{2}{3} - d_{12} \tag{4.37}$$

then, duty ratios d_{21} and d_{22} are

$$d_{21} = \frac{\frac{1}{3}(v_a^2 + v_b^2 + v_c^2) - \frac{V_g}{2}v_a}{v_a^2 + v_b^2 + v_c^2} \tag{4.38}$$

$$d_{22} = \frac{\frac{1}{3}(v_a^2 + v_b^2 + v_c^2) - \frac{V_g}{2} v_b}{v_a^2 + v_b^2 + v_c^2} \tag{4.39}$$

The analog circuit to solve Equations (4.35), (4.36), (4.38), and (4.39) is shown in Figure 4-8, in which six multipliers and four first-order LPWM circuits are used.

The three-phase boost inverter shown in Figure 4-2 is simulated with the LPWM circuit shown in Figure 4-8 in Saber. The control voltage is $v_a = V_m \sin(\Omega t)$ with V_m = 262 V and $\Omega = 2\pi(60\text{Hz})$. The LPWM circuit is implemented by four first-order LPWM circuits. The simulation results of output and control voltages as shown in Figure 4-9 imply that the output voltages are able to track the control voltages linearly. The difference in the amplitude and in the phase of the output voltages originates from the reactive components.

In summary, the three-phase converter can be linearized by first-order LPWM circuits. The switching instants of the switches are determined by integrators in the LPWM. The input signals of the PWM circuit, called the P function and Q function, are normally the nonlinear functions of the input and output voltage in three-phase converters. Analog implementation of these nonlinear function involves multipliers/dividers, making it complicated and not practical. However, if the P function and Q function are linear functions of input and control voltages, the LPWM modulator for three-phase converter can be implemented by first-order LPWM circuits without using multipliers or dividers [59, 60].

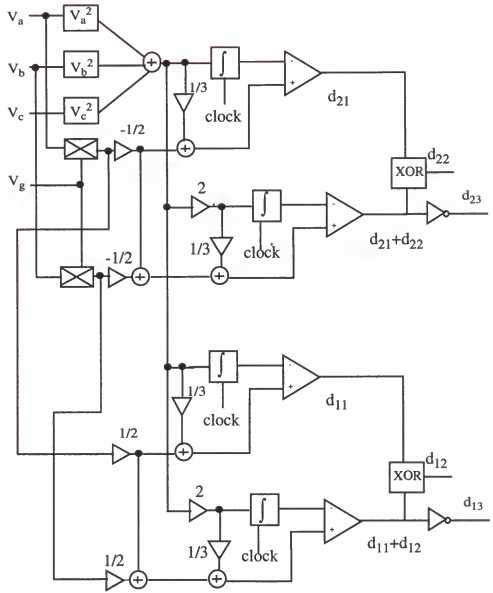


Figure 4-8 The LPWM implemented by the first-order LPMW circuits for a three-phase boost inverter.

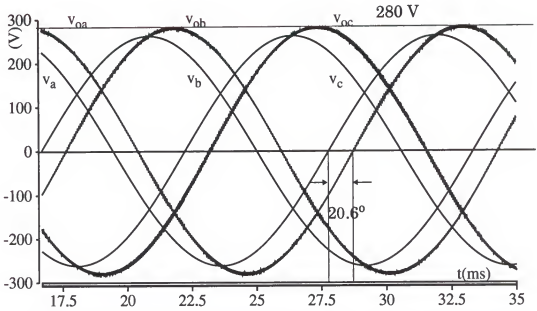


Figure 4-9 The simulation results of output and control voltages of the three-phase boost inverter controlled by first-order LPWM circuits. $v_a = V_m \sin(\Omega t)$ with V_m = 262 V and $\Omega = 2\pi(60\text{Hz})$.

4.5 Linearization by High-Order LPWM

The main problem for first-order LPWM circuits to linearize three-phase converters is that multipliers/dividers may be employed to synthesize the inputs to the integrators. The problem is solved by a technique presented in this section. With the help of this technique, the SFA equations of a three-phase converter are reduced into a set of SFA equations that have only one unknown duty ratio in each of them, and they have coefficients of linear functions of the control voltages. Different from the first-order LPWM implementation, this technique does not need to find the expressions of duty ratios,

and P and Q functions, and it synthesizes the LPWM directly from the reduced SFA equations. The resulting LPWM circuit is called high-order LPWM because it uses more than one integrators to get one duty ratio. The analog high-order LPWM modulator is developed for a general PWM converter in this section. It employs only integrators (with reset and hold) to compute the commutation instants of the switches. The inputs to the integrators and comparators are linear functions of the control and input voltages. The synthesis procedure of the high-order LPWM is demonstrated through a three-phase boost inverter. The modulator, together with the inverter, is simulated in Saber. The result shows that the output voltages can track the control voltages linearly, and the high-order LPWM modulator is simple and easy to use.

The synthesis of the high-order LPWM is based on the steady-state SFA equations of the PWM converter, which are just linear functions of state variables and duty ratios of the switches, as described in Chapter 2. In the steady-state condition, the derivative terms in state-space equations are zero. As an example, the steady-state SFA equations of a PWM converter with two independent duty ratios are given by

$$a_{11}d_{11} + a_{12}d_{12} = k_1 \tag{4.40}$$

$$a_{21}d_{11} + a_{22}d_{12} = k_2 \tag{4.41}$$

where coefficients a_{11} - a_{22}, k_1 and k_2 are related to control and input voltages. For the LPWM modulator, they are reference and input voltages.

As we know, the duty ratios d_{11} and d_{12} are slowly varying sinusoidal signals. When the switching frequency is sufficiently high, the value of the duty ratio in the current switching cycle can be assumed equal to the value in the last cycle:

$$d_{11}{}^{n-1} \cong d_{11}{}^{n} \tag{4.42}$$

$$d_{12}{}^{n-1} \cong d_{12}{}^{n} \tag{4.43}$$

where the superscript n stands for the current cycle, n-1 for the last cycle.

Substitution of Equations (4.42) and (4.43) into (4.40) and (4.41) yields:

$$a_{12}d_{12}^{n} = k_1 - a_{11}d_{11}^{n-1} \tag{4.44}$$

$$a_{21}d_{11}^{n} = k_2 - a_{22}d_{12}^{n-1} \tag{4.45}$$

where $a_{22}d_{12}^{n-1}$ and $a_{11}d_{11}^{n-1}$ are sampled and held during the previous switching cycle. They are available to solve d_{12} and d_{11}, respectively, during the current cycle. Since the switching frequency is assumed sufficiently high, and the control and input voltages vary slowly, all the coefficients in Equations (4.44) and (4.45), including $a_{22}d_{12}^{n-1}$ and $a_{11}d_{11}^{n-1}$, can be treated as constant.

Obviously, if d_{11} and d_{12} are solved directly from (4.40) and (4.41), their expressions are nonlinear functions of a_{11} - a_{22}, k_1, and k_2, namely, control voltages. Using integrators to solve these functions would involve nonlinear inputs to the integrators and multipliers/dividers in the resulting LPWM circuit, as shown in Figure 4-8. In contrast, the coefficients in Equations (4.44) and (4.45), a_{11} - a_{22}, k_1, and k_2, are linear functions of control voltages. Using

integrators to solve these equations involves only linear inputs to the integrators. Thus, the resulting circuitry would not require multipliers/dividers to synthesize the nonlinear inputs to the modulator circuits, making analog implementation much easier.

In order to use analog circuits to synthesize Equations (4.44) and (4.45), these equations are transformed into the integration forms:

$$\frac{1}{T_s}\int_0^{T_s d_{12}^n} a_{12}dt = k_1 - a_{11}d_{11}^{n-1} \tag{4.46}$$

$$\frac{1}{T_s}\int_0^{T_s d_{11}^n} a_{21}dt = k_2 - a_{22}d_{12}^{n-1} \tag{4.47}$$

The duty ratio d_{11} can be obtained by comparing the integration of a_{21} with $k_2 - a_{22}d_{12}^{n-1}$ through an integrator and a comparator. The duty ratio d_{12} can be solved in the same way. However, to do so, $a_{22}d_{12}^{n-1}$ and $a_{11}d_{11}^{n-1}$ on the left side of the equations should be available. Note that

$$\frac{1}{T_s}\int_0^{T_s d_{11}} a_{11}dt \approx a_{11}d_{11} \tag{4.48}$$

$$\frac{1}{T_s}\int_0^{T_s d_{12}} a_{22}dt \approx a_{22}d_{12} \tag{4.49}$$

Then these sampled terms can be implemented by the integrator with reset and hold, as shown in Figure 4-10. The integrator starts to integrate a_{11} after reset by the RESET signal. At the moment $d_{11}T_s$, the integration is stopped by the HOLD signal. The output of the integrator is held at the value of $a_{11}d_{11}$,

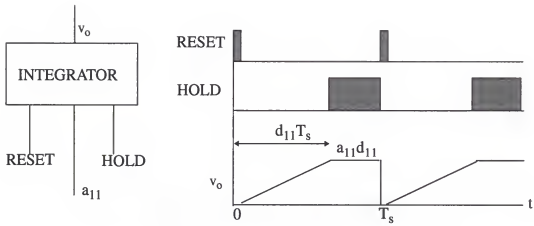


Figure 4-10 The integrator with reset and hold.

which will be available for the next switching cycle. The signal $a_{22}d_{12}$ can be generated in the same way.

From Equations (4.46) - (4.49) and the integrator shown in Figure 4-10, the high-order LPWM circuit can be synthesized, as shown in Figure 4-11. Its operation waveforms are shown in Figure 4-12. When the clock signal comes, the bottom integrators, #1 and #2, start to integrate their input signals a_{11} and a_{21}. As soon as integrator output v_{o2}, the integration of a_{21}, reaches $k_2 - a_{22}d_{12}^{n-1}$, the comparator produces a pulse S_1 with the duty ratio of d_{11}^n. This pulse resets the top integrators, #3 and #4, and provides the HOLD signal for integrator #1. Thus, the integrator output v_{o1} is held at the value of $a_{11}d_{11}^n$, which will be used to solve a_{12}. After reset, two integrators #3 and #4 on the top start to integrate a_{12} and a_{22}. As soon as integrator output v_{o4}, the integration of a_{12}, reaches $k_1 - a_{11}d_{11}^n$, the comparator generates a pulse S_2 with the duty ratio of d_{12}^n. This pulse provides the HOLD signal for #3

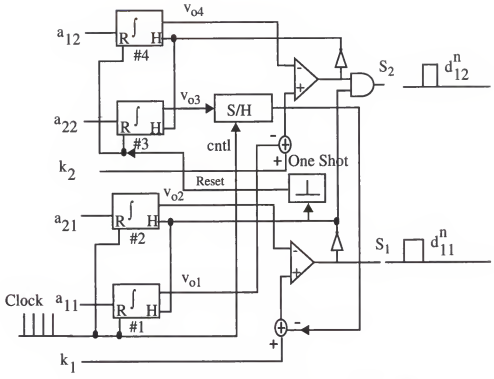


Figure 4-11 The high-order Linearizing PWM.

integrator. The integrator output v_{o3} is thus held at the value of $a_{22}d^n_{12}$, which will be used to solve d_{11} in the next cycle. The reset signal for the top integrators is generated by a one-shot circuit. To prevent changes in the integrator output v_{o3} from affecting the solution of duty ratio d_{11}, an extra sample/hold circuit is added to the PWM circuit. The AND gate in the circuit is used to disable the top comparator when solving for the duty ratio d_{11}.

As an example, a three-phase boost inverter, as shown in Figure 4-7, is controlled and linearized by the high-order LPWM circuit in Figure 4-11. The space-vector modulation (SVM) discussed in Chapter 3 is applied in this converter. In the SVM, the three-phase voltages v_a, v_b, and v_c are divided into six

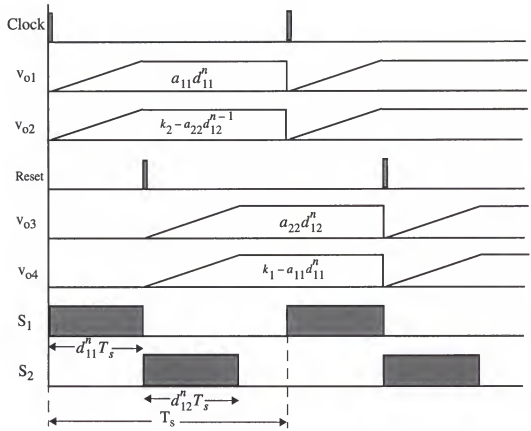


Figure 4-12 Waveforms of the high-order LPWM.

segments as shown in Figure 4-13. In each segment, one SPTT switch in Figure 4-7 is permanently attached to one of the three capacitors as the other sweeps through all three. The position of the stationary switch as well as the sweeping ones are determined by a six-stepped sequence.

In the first segment, 0^0-60^0, $v_b < v_a$ and $v_b < v_c$. Let $d_{22} = 1$, and $d_{21} = d_{23} = 0$, that is, S_{22} is on while S_{21} and S_{23} are off all the time during this segment. The switches, S_{11}, S_{12} and S_{13}, are switched at high switching frequency. In steady state, the averaged state-space equations are

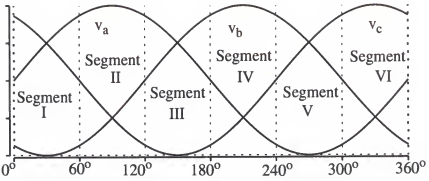


Figure 4-13 Balanced three-phase voltages.

$$0 = V_g - (d_{11} - d_{21})v_a - (d_{12} - d_{22})v_b - (d_{13} - d_{23})v_c \tag{4.50}$$

$$0 = (d_{11} - d_{21})i_L - \frac{2v_a - v_b - v_c}{3R} \tag{4.51}$$

$$0 = (d_{12} - d_{22})i_L - \frac{2v_b - v_a - v_c}{3R} \tag{4.52}$$

During the first segment,

$$d_{21} = d_{23} = 0 \tag{4.53}$$

$$d_{22} = 1 \tag{4.54}$$

Substituting Equations (4.53) and (4.54) into (4.50) - (4.52) and applying simple algebra, the steady-state equations for the first segment can be transformed as

$$V_g = d_{11}v_{ab} + d_{13}v_{cb} \tag{4.55}$$

$$(2d_{11} + d_{13})v_{cb} = (2d_{13} + d_{11})v_{ab} \tag{4.56}$$

From Equations (4.55) and (4.56), duty ratios d_{11}, d_{13}, and d_{12} can be solved by the high-order LPWM. Note that the output voltages will track the

reference voltages v_a, v_b, and v_c linearly when the boost inverter is controlled by the LPWM to solve Equations (4.55) and (4.56). In other words, the inverter would have low-distortion sinusoidal waveforms at the output, and nonlinearity of the boost type inverter is eliminated.

If the steady-state equations for the six segments are listed, one can see that they have the same forms as Equations (4.55) and (4.56). Thus, they can be expressed as a general form as follows:

$$V_g = d_x v_x + d_y v_y \tag{4.57}$$

$$(2d_x + d_y)v_y = (2d_y + d_x)v_x \tag{4.58}$$

$$d_z = 1 - d_x - d_y \tag{4.59}$$

where V_g is the dc input voltage of the inverter.

The coefficients v_x and v_y in Equations (4.57) and (4.58) are the reference voltage signals to the LPWM. They are six-stepped piecewise sinusoidal line-to-line voltages, as shown in Figure 4-14. Within different six-stepped segments, v_x and v_y takes different line-to-line voltages, as shown in Table 4.1, which are synthesized from continuous three-phase reference signals v_a, v_b, and v_c. The outputs of the modulator are PWM signals with duty ratios d_x, d_y, and d_z. For each segment of the SVM, d_x, d_y, and d_z, are assigned to three switches of the inverter based on Table 4.1. During the first segment, for instance, $d_x = d_{11}$, $d_y = d_{13}$, $d_z = d_{12}$. The positions of d_x and d_y over one complete period are shown in Table 4.1.

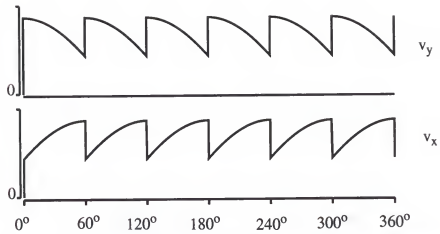


Figure 4-14 Six-stepped reference voltage signals to the LPWM.

Table 4.1 Six-step reference voltages and duty ratios.

	v_x	v_y	d_x	d_y	d_z	"1"	"0"	"0"
Seg. I	v_{ab}	v_{cb}	d_{11}	d_{13}	d_{12}	d_{22}	d_{23}	d_{21}
Seg. II	v_{ac}	v_{ab}	d_{23}	d_{22}	d_{21}	d_{11}	d_{12}	d_{13}
Seg. III	v_{bc}	v_{ac}	d_{12}	d_{11}	d_{13}	d_{23}	d_{21}	d_{22}
Seg. IV	v_{ba}	v_{bc}	d_{21}	d_{23}	d_{22}	d_{12}	d_{13}	d_{11}
Seg. V	v_{ca}	v_{ba}	d_{13}	d_{12}	d_{11}	d_{21}	d_{22}	d_{23}
Seg. VI	v_{cb}	v_{ca}	d_{22}	d_{21}	d_{23}	d_{13}	d_{11}	d_{12}

In order to use the proposed high-order LPWM, it is necessary to transform the preceding equations into the following forms:

$$d_y^n v_y = V_g - d_x^{n-1} v_x \tag{4.60}$$

$$d_x^n v_y = \frac{1}{2}(d_x^{n-1} v_x) + \frac{1}{2} d_y^n (2v_x - v_y) \tag{4.61}$$

Comparing Equations (4.60) and (4.61) with (4.44) and (4.45), it is not difficult to find

$$a_{12} = v_y \tag{4.62}$$

$$a_{22} = v_x \tag{4.63}$$

$$a_{21} = v_y \tag{4.64}$$

$$a_{11} = 2v_x - v_y \tag{4.65}$$

$$k_1 = V_g \tag{4.66}$$

$$k_2 = d_x^{n-1} v_x^{n-1} \tag{4.67}$$

Replacing the inputs of the high-order LPWM in Figure 4-11 with the six-step reference voltages in Equations (4.62) - (4.66), the high-order LPWM for the three-phase boost inverter is then synthesized, as shown in Figure 4-15. It is worth noting that the inputs to the integrators are linear functions of the reference and input voltages, and analog implementation of which involves only adders/subtractors, as shown in Figure 4-15.

The three-phase boost inverter, as shown in Figure 4-2, is simulated with the proposed high-order LPWM circuit shown in Figure 4-15 in Saber. The control voltage is $v_a = V_m \sin(\Omega t)$ with V_m = 262 V and $\Omega = 2\pi(60\text{Hz})$. The inputs of the LPWM circuit in Figure 4-15 are the six-step reference signals v_x and v_y, which are generated from v_a, v_b, and v_c. The circuits that generate six-step reference signals are not shown here, but they can be easily built in Saber by some analog switches and some comparators. The waveforms of v_x

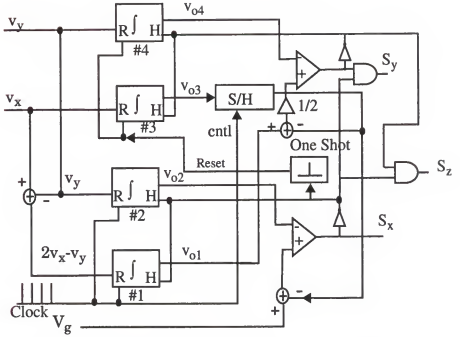


Figure 4-15 The high-order LPWM for three-phase boost inverter.

and v_y are shown in Figure 4-14. The outputs of the LPWM circuits are the PWM signal d_x, d_y, and d_z. They will be assigned to the six switches S_{11} - S_{23}, according to Table 4.1, by the encoding circuits. This circuit can be implemented, according to Table 4.1, by logic circuits. One of the simple encoding circuits is given in Chapter 6. The simulation results shown in Figure 4-16 are the output and control voltages. Output voltages in Figure 4-16 are supposed to equal control voltages according to the theory of the LPWM synthesis. However, the simulation shows that the amplitude of output voltages is a little higher than that of control voltages, and there is a phase shift between output and control voltages. This phenomenon is because of the reactive components in the power converter, which will be explained in detail in Chapter 5. The

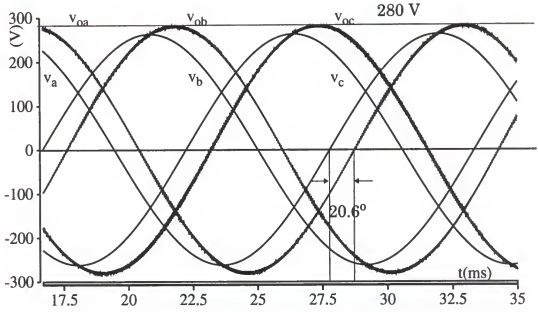


Figure 4-16 The simulation results of output and control voltages of the three-phase boost inverter controlled by the high-order LPWM circuit. $v_a = V_m \sin(\Omega t)$ with V_m = 262 V and $\Omega = 2\pi(60\text{Hz})$.

simulation results for the integrator outputs and the outputs of the high-order LPWM circuit are shown in Figure 4-17.

Over the one sinusoidal cycle, the switching signals for six switches in the inverter are shown in Figure 4-18. It shows that each switch in the inverter operates at high frequency and low frequency alternatively. The duty ratios d_{11} - d_{23} for six switches can be obtained by taking the average of the switching functions in the Saber. The results are shown in Figure 4-19. The duty ratios of the SVM, solved by the high-order LPWM, are piecewise sinusoids, similar with the piecewise sinusoidal modulation waveforms described for the conventional SVM method in Chapter 3. However, their amplitudes are

different. The modulation amplitude of the conventional SVM is proportional to the control voltage, where as the amplitude of the duty ratios generated by LPWM is a nonlinear function of the control and input voltages.

In conclusion, most three-phase PWM converters have nonlinear control-to-output relationships that make the output voltages unable to track the control voltages linearly when they are controlled by the conventional PWM modulator. The first-order LPWM modulator can be used to linearize the three-phase converter, but it may involve multipliers/dividers to synthesize the inputs to the integrators, as long as there are nonlinear terms of control voltages in the expressions of duty ratios.

The technique presented in this chapter is able to reduce the SFA equations of the converter into a set of SFA equations that have only one unknown duty ratio in each of them. The coefficients of these SFA equations are just linear functions of the control voltages. The PWM circuit synthesized from these SFA equations, called high-order LPWM, uses only integrators (with reset and hold) to compute switching instants of the switches. The inputs to integrators are just linear functions of control and input voltages. A high-order LPWM is synthesized and simulated for a three-phase boost inverter. The results show that the output voltages can track the control voltage linearly. The control circuit is simple and easy to use.

The synthesis technique of the high-order LPWM modulator is developed for a three-phase boost inverter here, but it may be extended to all the three-phase converters or multi-phase PWM converters.

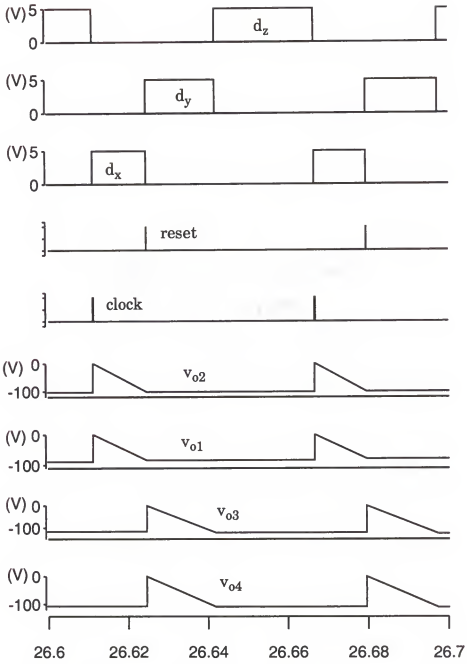


Figure 4-17 The simulation results for integrator outputs and the LPWM outputs.

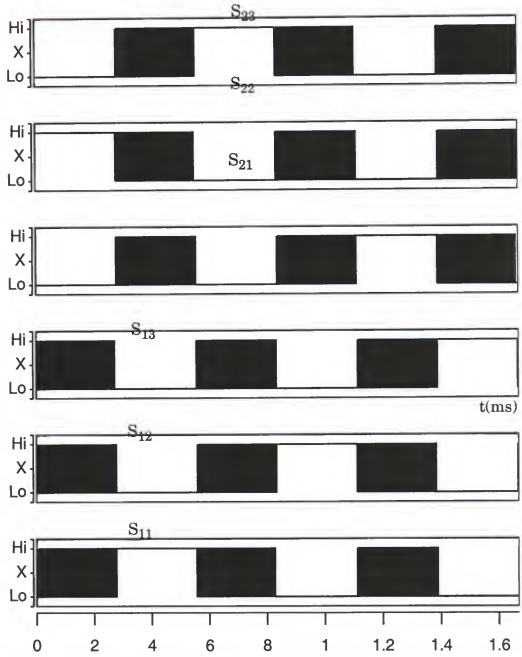


Figure 4-18 The switching signals of six switches in the inverter over the complete sinusoidal period.

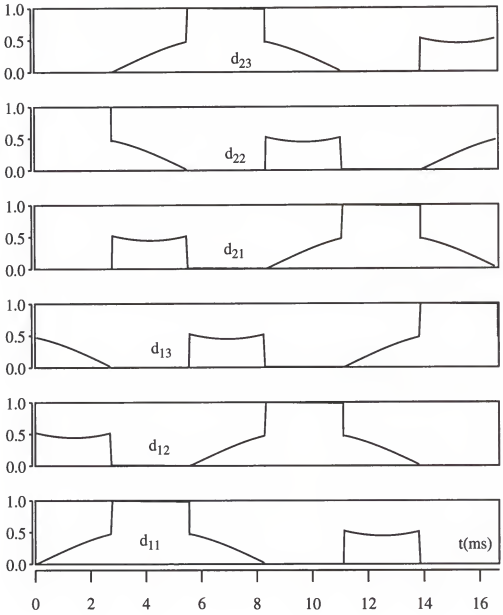


Figure 4-19 The simulation results of the duty ratios for the six switches in the inverter.

CHAPTER 5
ANALYSIS OF HIGH-ORDER LINEARIZING PULSEWIDTH MODULATOR

This chapter analyzes the high-order linearizing pulsewidth modulator (LPWM) for a balanced three-phase boost inverter. In the first section, the sampling effects of the high-order LPWM are neglected for simplicity. The duty ratios of the output PWM signals of the modulator are shown as balanced three-phase sinusoids, and their amplitudes are inversely proportional to the amplitude of the control voltages. The output voltages of the inverter equal the control voltages multiplied by a constant gain. The nonlinearity of the three-phase boost inverter is eliminated by the high-order LPWM. Meanwhile, line voltage regulation is improved because the output voltages of the inverter are mainly controlled by the control voltages.

The sampling effects of the high-order LPWM are discussed in Section 2. A pole is contributed by the sampling effects. The location of this pole is determined by the sampling frequency. When the sampling frequency is high, the bandwith of the modulator is wide. Simulation results show that the modulator is able to follow change in the control voltage within one switching cycle. Therefore, sampling effects of the modulator can be neglected in the design.

5.1 Analysis of High-Order Linearizing PWM

5.1.1 Modeling the High-Order LPWM

A balanced three-phase boost inverter with the high-order LPWM is shown in Figure 5-1. According to discussions in Section 4.5 of Chapter 4, the modulation equations to synthesize the high-order LPWM modulator are given by

$$V_{gr} = d_{11}v_{ab} + d_{13}v_{cb} \tag{5.1}$$

$$(2d_{11} + d_{13})v_{cb} = (2d_{13} + d_{11})v_{ab} \tag{5.2}$$

$$d_{12} = 1 - d_{11} - d_{13} \tag{5.3}$$

where d_{11}, d_{13}, and d_{12} are duty ratios of the PWM signals for the switches S_{11}, S_{13}, and S_{12}, respectively; v_{cb} and v_{ab} are line-to-line voltages obtained from the control voltages v_a, v_b, and v_c; and V_{gr} is sampled from input voltage

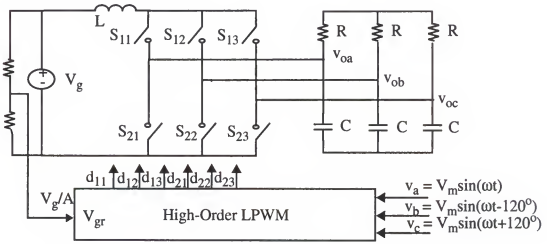


Figure 5-1 The LPWM controlled three-phase boost inverter.

V_g by a voltage divider. The ratio of the voltage divider is A, then V_{gr} is given by:

$$V_{gr} = \frac{V_g}{A} \tag{5.4}$$

The ratio A is big enough so that V_{gr} could not saturate the operational circuit in the analog high-order LPWM. Similarly, the amplitude of the control voltages, V_m, must be small enough, so that the control voltages would not saturate the operational circuit in the LPWM.

The modulation equations (5.1) and (5.2) are derived from the first segment of space-vector modulation (SVM). In the first segment of the SVM, duty ratios $d_{21} = d_{23} = 0$, $d_{22} = 1$. Thus, the duty ratios d_{11}, d_{13} and d_{12} can be replaced by the effective duty ratios d_a, d_c and d_b. Then, the modulation equations (5.1) and (5.2) become

$$V_{gr} = d_a v_{ab} + d_c v_{cb} \tag{5.5}$$

$$(2d_a + d_c)v_{cb} = (2d_c + d_a)v_{ab} \tag{5.6}$$

$$d_b = -d_a - d_c \tag{5.7}$$

In fact, as shown in the above equations, only effective duty ratios play a role of modulation.

For the high-order LPWM, V_{gr}, v_{ab}, and v_{cb} in Equations (5.5) and (5.6) are known. The task of the high-order LPWM is to solve d_a, d_c and d_b from Equations (5.5) - (5.7). By applying a simple algebra to Equations (5.5) - (5.7), d_a, d_b, and d_c can be expressed as the functions of v_a, v_b, and v_c:

$$d_a = \frac{3}{2}\frac{V_g}{A}\frac{v_a}{v_a^2 + v_b^2 + v_c^2 - v_a v_b - v_a v_c - v_c v_b} \tag{5.8}$$

$$d_b = \frac{3}{2}\frac{V_g}{A}\frac{v_b}{v_a^2 + v_b^2 + v_c^2 - v_a v_b - v_a v_c - v_c v_b} \tag{5.9}$$

$$d_c = \frac{3}{2}\frac{V_g}{A}\frac{v_c}{v_a^2 + v_b^2 + v_c^2 - v_a v_b - v_a v_c - v_c v_b} \tag{5.10}$$

For a balanced three-phase system,

$$v_a^2 + v_b^2 + v_c^2 - v_a v_b - v_a v_c - v_c v_b = \frac{9}{4}V_m^2 \tag{5.11}$$

where V_m is the amplitude of the balanced three-phase voltages. Substitution of Equation (5.11) into (5.8) - (5.10) yields the effective duty ratios:

$$\boldsymbol{d} = \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} d_{11} - d_{21} \\ d_{12} - d_{22} \\ d_{13} - d_{23} \end{bmatrix} = \begin{bmatrix} \frac{2V_g}{3AV_m}\sin(\omega t) \\ \frac{2V_g}{3AV_m}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ \frac{2V_g}{3AV_m}\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{5.12}$$

The effective duty ratios of the PWM signals in Equation (5.12) are balanced three-phase sinusoids. The amplitude of the sinusoids is inversely proportional to the amplitude of control voltages.

The model of the high-order LPWM, as shown in (5.12), is derived in the *abc* coordinates. Its model in the *ofb* coordinates can be obtained by applying *abc-ofb* transformation, as described in Chapter 2, to Equation (5.12). In the derivation, assume that all the initial phases relative to the transformation

matrix **T** and duty ratio vector **d** are zero. The resulting time-invariant *ofb* model of the high-order LPWM is

$$D_{ofb} = [D_o \; D_f \; D_{bw}]^T = \left[0 \;\; \frac{V_g}{\sqrt{3}AV_m} \;\; \frac{V_g}{\sqrt{3}AV_m}\right]^T \tag{5.13}$$

The zero-sequence component of the effective duty ratios is zero; the forward- and backward-sequence components become the same:

$$D_e = D_f = D_{bw} = \frac{V_g}{\sqrt{3}AV_m} \tag{5.14}$$

The small-signal model of the high-order LPWM can be obtained by perturbation of (5.14) around a dc operating point specified by the input voltage V_g, the control voltage V_m, as well as the effective duty ratio D_e. The small-signal component of the duty ratio $\hat{d}_e$ becomes a linear combination of the small-signal perturbations in V_g and V_m:

$$\hat{d}_e = K_m \hat{v}_m + K_g \hat{v}_g \tag{5.15}$$

The gain K_m and K_f are found by differentiation of (5.15) with respect to V_g and V_m:

$$K_m = \frac{\hat{d}_e}{\hat{v}_m} = -\frac{1}{\sqrt{3}AV_m^2}\frac{V_g}{} = -\frac{D_e}{V_m} \tag{5.16}$$

$$K_g = \frac{\hat{d}_e}{\hat{v}_g} = \frac{1}{\sqrt{3}AV_m}\frac{1}{} \tag{5.17}$$

5.1.2 Steady-State Analysis

In this section, the output voltages of the three-phase boost inverter that is controlled by the high-order LPWM will be derived. From Equation (3.32) of Chapter 3, the amplitude of the output voltages of SVM three-phase boost inverter is given by

$$V_{om} = \frac{2}{3}\frac{V_g}{D_m}\sqrt{1+(\omega RC)^2} \tag{5.18}$$

D_m in Equation (5.18) is provided by the high-order LPWM that is given by:

$$D_m = \frac{2V_g}{3AV_m} \tag{5.19}$$

Then, the amplitude V_{om} of the output voltages becomes

$$V_{om} = AV_m\sqrt{1+(\omega RC)^2} \tag{5.20}$$

Of course, this result can be obtained by combining the steady-state *ofb* equivalent circuit of the three-phase boost inverter, as shown in Figure 2-14 of Chapter 2, and the *ofb* model of the modulator, as shown in Equation (5.14). The resulting *ofb* equivalent circuit is shown in Figure 5-2. The resistors in Figure 5-2 are reflected to the primary side of the transformers. The voltage V_{bw} is then solved by the voltage divider as following:

$$V_{bw} = \frac{1}{2D_e}V_g(1-j\Omega RC) \tag{5.21}$$

Substitution of D_e in Equation (5.14) into Equation (5.21) yields

$$V_{bw} = \frac{\sqrt{3}}{2}AV_m(1-j\Omega RC) \tag{5.22}$$

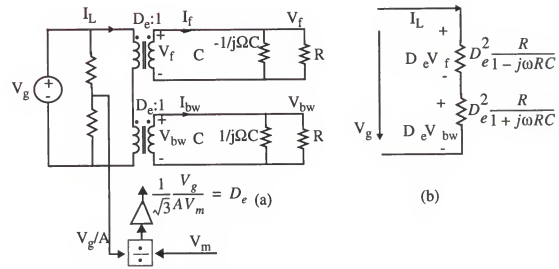


Figure 5-2 (a) The steady-state *ofb* equivalent circuit of the LPWM-controlled three-phase boost inverter; (b) its simplified circuit.

The output voltage phasor $\mathbf{V_o}$ is given by

$$V_o = V_m(1 - j\Omega RC) \tag{5.23}$$

From Equation (5.23), one can easily find that the amplitude of the output voltages is given by

$$V_{om} = AV_m\sqrt{1 + (\omega RC)^2} \tag{5.24}$$

which is the same as Equation (5.20). The output voltages have a phase shift from the control voltages that is determined by

$$\angle v_{oa} = tan^{-1}(\omega RC) \tag{5.25}$$

As a conclusion, the high-order LPWM can make the output voltages of the three-phase boost inverter track the control voltages linearly, independent of the operating condition of the inverter, as shown in Equation (5.24). The

line voltage regulation is improved because the output voltages are mainly determined by control voltage and a constant gain set by the voltage divider. A phase shift between the control and output voltages is caused by the load resistance and filter capacitor.

5.1.3 Small-Signal Analysis

This section discusses the small-signal property of the LPWM-controlled three-phase boost inverter. Its small-signal equivalent circuit is shown in Figure 5-3 that is the combination of the small-signal model of the modulator, as shown in Equation (5.15), and the *ofb* small-signal equivalent circuit of three-phase boost inverter, as shown in Figure 2-18 of Chapter 2.

Let $\hat{v}_g = 0$, the control-to-output transfer function of the power stage is shown in Equation (2.64) of Chapter 2 and given by

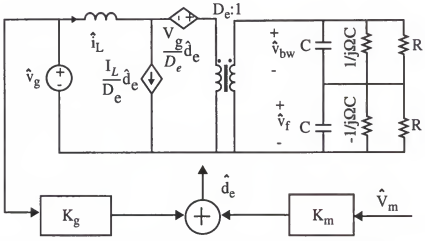


Figure 5-3 The small-signal model of the LPWM controlled three-phase boost inverter in the *ofb* coordinates.

$$G(s) = \frac{\hat{v}_{om}}{\hat{d}_e} = -\frac{V_g}{2D_e^2}\sqrt{1+\left(\frac{\Omega}{\omega_p}\right)^2}\frac{\left(1-\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_{z1}}\right)}{D(s)} \tag{5.26}$$

Combined with transfer function K_m of the modulator, the control-to-output transfer function G_c of the LPWM-controlled three-phase boost inverter is given by

$$G_c(s) = \frac{\hat{v}_{om}}{\hat{v}_m} = \frac{\hat{v}_{om}}{\hat{d}_e} \bullet \frac{\hat{d}_e}{\hat{v}_m} = G(s)K_m = \frac{\sqrt{3}}{2}A\sqrt{1+\left(\frac{\Omega}{\omega_p}\right)^2}\frac{\left(1-\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_{z1}}\right)}{D(s)} \tag{5.27}$$

Therefore, at the low frequency, the small-signal control-to-output gain is a constant A, independent of operating conditions, which can simplify feedback-loop design of the LPWM-controlled power converter. It is to note that the LPWM does not have any effect on corner frequencies of the transfer function. These corner frequencies remains the same as those in the conventional-PWM-controlled inverter.

Let $\hat{d}_e = 0$, the input-to-output transfer function of the power stage is shown in Equation (2.66) of Chapter 2 and given by

$$H(s) = \frac{\hat{v}_{om}}{\hat{v}_g} = \frac{1}{2D_e}\sqrt{1+\left(\frac{\Omega}{\omega_p}\right)^2}\frac{\left(1+\frac{s}{\omega_{z1}}\right)}{D(s)} \tag{5.28}$$

From Equations (5.26) and (5.28), one can find that

$$G(s) = -\frac{V_g}{D_e}\left(1-\frac{s}{\omega_z}\right)H(s) \tag{5.29}$$

From Figure 5-3, the input-to-output transfer function of the LPWM-controlled three-phase boost inverter can be expressed by

$$H_L(s) = H(s) + K_g G(s) \tag{5.30}$$

To simplify the derivation, K_g in (5.17) is expressed by D_e and V_g

$$K_g = \frac{D_e}{V_g} \tag{5.31}$$

Substituting (5.29) and (5.31) into (5.30), then H_L can be found as

$$H_L(s) = H(s) - \frac{D_e}{V_g} \bullet \frac{V_g}{D_e}\left(1 - \frac{s}{\omega_z}\right)H(s) = \frac{s}{\omega_z}H(s) \tag{5.32}$$

The results in Equation (5.32) show that the input-to-output transfer function H_L is ideally zero at dc when the three-phase boost inverter is controlled by the high-order LPWM. Compared with the three-phase boost inverter without the LPWM control, as shown in Equation (5.28), the audiosusceptibility of the LPWM-controlled three-phase boost inverter, as shown in (5.32), is significantly reduced.

To appreciate this improvement, we use LPWM and conventional PMW to control three-phase boost inverter separately, and compare the amplitudes of output voltages in both cases. The simulation results are shown in Figure 5-4. According to simulation results, the steady-state amplitude of output voltages, controlled by conventional PWM, would vary with the input voltage; however, the steady-state amplitude of output voltages, controlled by the LPWM, would not be affected by the input voltage.

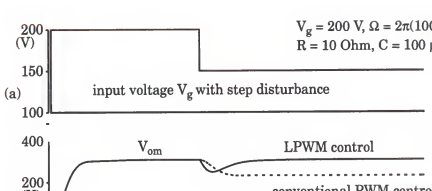


Figure 5-4 (a) input voltage; (b) amplitudes of output voltages controlled by LPWM, and by conventional PWM.

5.2 Sampling Effects in High-Order LPWM

5.2.4 Modeling the High-Order LPWM with Sampling Effects

This section discusses modeling of the high-order LPWM that includes sampling effects. Considering the sampling effects, the modulation equations to synthesize the high-order LPWM modulator are given by

$$d_{13}^n v_{cb} = V_{gr} - d_{11}^{n-1} v_{ab} \tag{5.33}$$

$$d_{11}^n v_{cb} = \frac{1}{2}(d_{11}^{n-1} v_{ab}) + \frac{1}{2} d_{13}^n (2v_{ab} - v_{cb}) \tag{5.34}$$

$$d_{12}^n = 1 - d_{11}^n - d_{13}^n \tag{5.35}$$

With the above modulation equations, the synthesis of the high-order LPWM by analog circuits will not involve multipliers/dividers that have been discussed in Section 4.5 of Chapter 4. In modulation equations (5.33) - (5.35), V_{gr}, v_{ab}, and v_{cb} are known. The task of modeling the high-order LPWM is to solve

d_{11}, d_{13} and d_{12} from Equations (5.33) - (5.35). From Equation (5.33), d_{13}^n can be expressed as

$$d_{13}^n = \frac{V_{gr} - d_{11}^{n-1} v_{ab}}{v_{cb}} \tag{5.36}$$

Substitution of Equation (5.36) into Equation (5.34) and applying simple algebra yields:

$$2d_{11}^n v_{cb}^2 = 2d_{11}^{n-1}(v_{ab}v_{cb} - v_{ab}^2) + V_{gr}(2v_{ab} - v_{cb}) \tag{5.37}$$

Adding $-2d_{11}^{n-1}v_{cb}^2$ to both sides of Equation (5.37), yields

$$d_{11}^n - d_{11}^{n-1} = d_{11}^{n-1}\frac{(v_{ab}v_{cb} - v_{ab}^2 - v_{cb}^2)}{v_{cb}^2} + V_{gr}\frac{(2v_{ab} - v_{cb})}{2v_{cb}^2} \tag{5.38}$$

Multiplying $\frac{1}{T_s}$ with Equation (5.38) and assuming

$$\frac{d_{11}^n - d_{11}^{n-1}}{T_s} \cong \frac{d}{dt}(d_{11}) \tag{5.39}$$

where d_{11} is a continuous function of time, Equation (5.38) then becomes a continuous differential equation:

$$\frac{d}{dt}(d_{11}) = d_{11}\frac{(v_{ab}v_{cb} - v_{ab}^2 - v_{cb}^2)}{v_{cb}^2 T_s} + V_{gr}\frac{(2v_{ab} - v_{cb})}{2v_{cb}^2 T_s} \tag{5.40}$$

From Equation (5.33), d_{13}^{n+1} can be expressed as

$$d_{13}^{n+1} v_{cb} = V_{gr} - d_{11}^n v_{ab} \tag{5.41}$$

Substitution of d_{11}^n in Equation (5.34) into (5.41) yields

$$d_{13}^{n+1} v_{cb}^2 = V_{gr} v_{cb} - \frac{1}{2} d_{11}^{n-1} v_{ab}^2 - \frac{1}{2} d_{13}^n (2v_{ab}^2 - v_{ab}v_{cb}) \tag{5.42}$$

Substitution of d_{11}^{n-1} in Equation (5.33) into (5.42) yields

$$d_{13}^{n+1} v_{cb}^2 = \frac{V_{gr}}{2}(2v_{cb} - v_{ab}) + d_{13}^{n}(v_{ab}v_{cb} - v_{ab}^2) \tag{5.43}$$

By adding $-d_{13}^{n} v_{cb}^2$ to both sides of Equation (5.43) and employing the assumption in Equation (5.39), the continuous differential equation for duty ratio d_{13} can be found as follows:

$$\frac{d}{dt}(d_{13}) = d_{13}\frac{(v_{ab}v_{cb} - v_{ab}^2 - v_{cb}^2)}{v_{cb}^2 T_s} + V_{gr}\frac{(2v_{cb} - v_{ab})}{2v_{cb}^2 T_s} \tag{5.44}$$

$$d_{12} = 1 - d_{11} - d_{13} \tag{5.45}$$

d_{11}, d_{13}, and d_{12} can be solved from Equations (5.40), (5.44), and (5.45). Note that these differential equations have included sampling effects.

5.2.5 Steady-State Analysis

Under steady-state condition, letting the derivative in Equation (5.40) be zero yields:

$$d_{11} = \frac{V_{gr}}{2}\frac{2v_{ab} - v_{cb}}{v_{ab}^2 + v_{cb}^2 - v_{ab}v_{cb}} = \frac{3V_{gr}}{2}\frac{v_a}{v_{ab}^2 + v_{cb}^2 - v_{ab}v_{cb}} = \frac{2}{3}\frac{V_g}{AV_m}\sin\theta \tag{5.46}$$

d_{13} is obtained from Equation (5.44) by letting the derivative be zero:

$$d_{13} = \frac{V_{gr}}{2}\frac{2v_{ab} - v_{cb}}{v_{ab}^2 + v_{cb}^2 - v_{ab}v_{cb}} = \frac{3V_{gr}}{2}\frac{v_c}{v_{ab}^2 + v_{cb}^2 - v_{ab}v_{cb}} = \frac{2}{3}\frac{V_g}{AV_m}\sin\left(\theta + \frac{2\pi}{3}\right) \tag{5.47}$$

where $v_{ab}^2 + v_{cb}^2 - v_{ab}v_{cb} = \frac{9}{4}V_m^2$ in the balanced three-phase voltages. The effective duty ratios can then be expressed as

$$\boldsymbol{d} = \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} d_{11} - d_{21} \\ d_{12} - d_{22} \\ d_{13} - d_{23} \end{bmatrix} = \begin{bmatrix} \frac{2V_g}{3AV_m}\sin(\theta) \\ \frac{2V_g}{3AV_m}\sin\left(\theta - \frac{2\pi}{3}\right) \\ \frac{2V_g}{3AV_m}\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \tag{5.48}$$

By comparing Equation (5.12) and Equation (5.48), a conclusion can be made. Under steady-state condition, the effective duty ratios that involve sampling effects are shown to be the same as those without sampling effects.

5.2.6 Small-Signal Analysis

This section discusses the dynamics of the high-order LPWM introduced by sampling. The dynamic study is restricted only to the small-signal sense. The angle θ of three-phase voltages in Equations (5.40) - (5.45) is assumed constant, thus, the coefficients in these equations become constant. The small-signal analysis will predict the response of the modulator to small perturbations around a quiescent operating point. Let the input and output of the modulator consist of a steady-state and a perturbed component:

$$v_m = V_m + \hat{v}_m \quad d_m = D_m + \hat{d}_m \quad v_{gr} = V_{gr} + \hat{v}_{gr} \tag{5.49}$$

where caret implies small-signal perturbations. Substitution of Equation (5.49) into Equation (5.40) and neglect of the steady-state and second-order terms then yield the following response for the duty ratio d_{11} in the Laplace domain:

$$\hat{d}_m(s) = K_m\hat{v}_m + K_g\hat{v}_g \tag{5.50}$$

$$K_m = \frac{\hat{d}_m}{\hat{v}_m} = -\frac{3}{2}\frac{V_g}{AB^2V_m^2T_sP(s)} \tag{5.51}$$

$$K_g = \frac{\hat{d}_m}{\hat{v}_g} = \frac{3}{2}\frac{A}{B^2V_mT_sP(s)} \tag{5.52}$$

where

$$B = \sin(\theta + 120^o) - \sin(\theta - 120^o) \tag{5.53}$$

$$P(s) = s + \frac{9}{4}\frac{1}{B^2T_s} \tag{5.54}$$

From the small-signal analysis, we can find that the sampling effects contribute a pole in the transfer functions of the high-order LPWM. The pole is related to the sampling frequency. Increase of the switching frequency will move away the pole and make the bandwidth wider. At s = 0, K_m and K_g are found as the follows:

$$K_m|_{s=0} = \frac{\hat{d}_m}{\hat{v}_m} = -\frac{2}{3}\frac{V_g}{AV_m^2} \tag{5.55}$$

$$K_g|_{s=0} = \frac{\hat{d}_m}{\hat{v}_g} = \frac{2}{3}\frac{A}{V_m} \tag{5.56}$$

Comparing the above equations with Equations (5.16) and (5.17), one can find that the gain K_m and K_g, derived without considering the sampling effects, are the dc gains of the transfer function of the high-order LPWM with sampling effects. When the sampling effects are involved, these gains reduce with the frequency.

The bandwidth of the high-order LPWM modulator is obtained from Equation (5.54):

$$f_{-3dB} = \frac{9}{8\pi} \frac{1}{(\sin(\theta + 120^o) - \sin(\theta - 120^o))^2 T_s} \tag{5.57}$$

The bandwidth is a function of sampling period T_s and angle θ. At $\theta = 0^o$, the bandwidth is the smallest, and the bandwidth is given by

$$f_{-3dB} = \frac{3}{8\pi} \frac{1}{T_s} \tag{5.58}$$

For f_s = 24 KHz, f_{-3dB} = 2.9 KHz. Given V_g = 5 V, V_m = 10 V, f_s = 24 KHz, A = 1, the frequency response of K_m of the high-order LPWM is shown in Figure 5-5. The -3dB bandwidth is shown around 2.9 KHz.

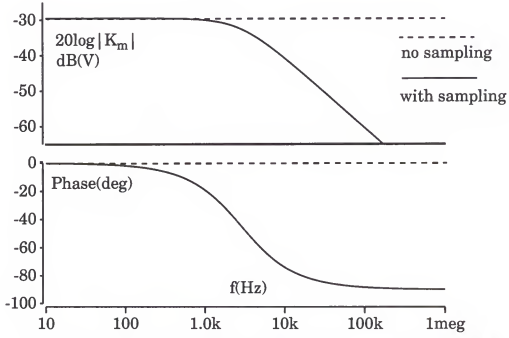


Figure 5-5 The frequency response of the high-order LPWM.

To appreciate how quick the high-order LPWM is, this LPWM is tested in Saber for the step response. The test circuit is shown in Figure 5-6. As shown in Figure 5-6, at $\theta = 0^o$, the amplitude of the reference signals jump from 10 V to 20 V, where the output of the modulator S_1, S_2, and S_3 are measured and shown in Figure 5-7. During the switching cycle before $\theta = 0^o$, the amplitude of control voltages is 10 V, resulting in the amplitude of duty ratios

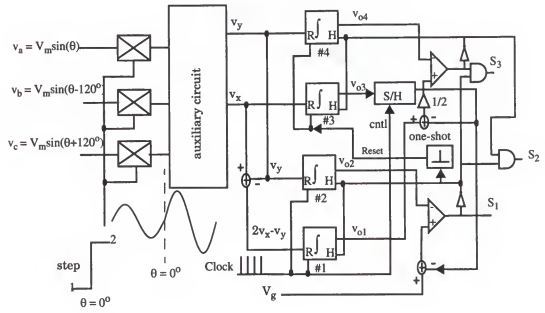


Figure 5-6 The circuit to test the step response of the high-order modulator. V_m = 10 V, V_g = 5 V, f_s = 24 KHz.

$D_m = 0.333$ according to Equation (5.48). The measured effective duty ratios of S_1, S_2, and S_3 are 0.0065, 0.29, and 0.295, respectively. According to

$$d_a^2 + d_b^2 + d_c^2 = \frac{3}{2}D_m^2 \tag{5.59}$$

The amplitude of effective duty ratios can be extracted as:

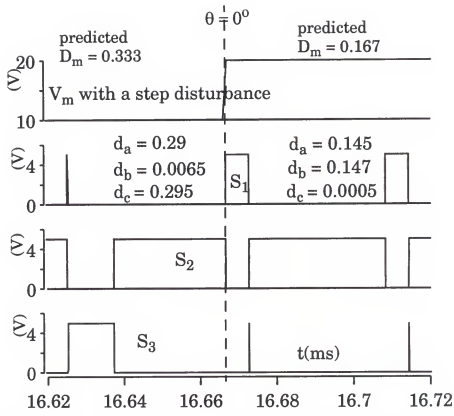


Figure 5-7 The simulation results of the step response of the high-order LPWM modulator.

$$D_m|_{0^{\circ}-} = 0.338 \tag{5.60}$$

During the switching cycle after $\theta = 0^{\circ}$, the amplitude of control voltages jumps to 20 V, resulting in the amplitude of duty ratios $D_m = 0.167$ according to Equation (5.48). The measured effective duty ratios of S_1, S_2, and S_3 are 0.145, 0.147, and 0.0005. Similarly, the amplitude of effective duty ratios is

$$D_m|_{0^{\circ}+} = 0.169 \tag{5.61}$$

Comparing Equations (5.60) and (5.61), one can find that the modulator is able to follow the step inputs very quickly, and it goes into steady-state condition within one switching cycle after step response.

In summary, the high-order LPWM is modeled and analyzed for a three-phase boost inverter. The sampling effects in the modulator contribute a pole that is determined by the switching frequency. This LPWM provides a wide bandwidth for the transfer function of the modulator. The modulator is able to react very quickly to the step input, and it goes into steady-state condition within one switching cycle according to step response measured in the simulation. For this reason, the delay caused by the sampling effects can be neglected when we analyze and design the high-order LPWM.

CHAPTER 6
IMPLEMENTATION AND EXPERIMENTAL RESULTS OF HIGH-ORDER LINEARIZING PULSEWIDTH MODULATOR

A high-order linearizing pulsewidth modulator (LPWM) is constructed to control a prototype three-phase boost inverter in this chapter. The whole test system is shown in Figure 6-1(a). The ideal switch in Figure 6-1(a) is implemented by a MOSFET and a diode, as shown in Figure 6-1(b). A passive snubber consisting of a capacitor and a resistor is put in parallel with the MOSFET to reduce di/dt noise and protect MOSFET from overheat. The PWM algorithm used for the inverter is space-vector modulation (SVM), also called six-step modulation, that is discussed in Section 3.4 of Chapter 3 and Section 4.5 of Chapter 4.

The reference circuit in Figure 6-1(a) generates balanced three-phase voltages from a single-phase signal v_a. It also provides two six-step reference voltages v_1 and v_2 for the high-order LPWM, and six-step signals S_{g1} - S_{g6} for gate-drive logic. The high-order LPWM in Figure 6-1(a) synthesizes PWM signals, S_1 - S_3, from the six-step reference v_1 and v_2, and input voltage V_g. It provides the PWM signals S_1 - S_3 to gate-drive logic. The gate-drive logic in Figure 6-1(a) assigns three PWM signals S_1 - S_3 to the six switches in the inverter based on the six-step signals S_{g1} - S_{g6}. Isolation circuits, MOSFET drivers, and floating power supplies are not included for simplicity.

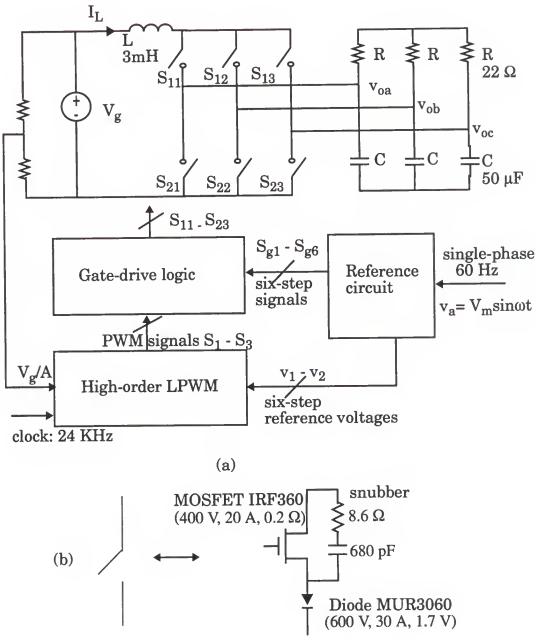


Figure 6-1 (a) The test system of a three-phase boost inverter controlled by the high-order LPWM; (b) ideal switch and its implementation in the inverter.

The analog high-order LPWM, the reference circuit, and the gate-drive logic in Figure 6-1(a) are presented in the first section of this chapter. The corresponding waveforms measured from the prototype circuits are also included. The second section presents experimental results and discusses how the high-order LPWM improves the performance of a nonlinear three-phase boost inverter. Some practical issues in the experiment are discussed in the last section.

6.1 Analog Implementation of High-Order LPWM

The high-order LPWM synthesizes the PWM signals S_1, S_2, and S_3 from the six-step reference voltages, v_1 and v_2, and input voltage V_g, as shown in Figure 6-1(a). The circuit that generates v_1 and v_2 consists of three parts. The first part is to generate three-phase reference voltages from a single-phase voltage. The second part is to generate digital six-step signals S_{g1} - S_{g6}. The third part is to produce the six-step reference voltages v_1 and v_2 using analog multiplexers. The circuit in Figure 6-2 takes a single-phase voltage v_a

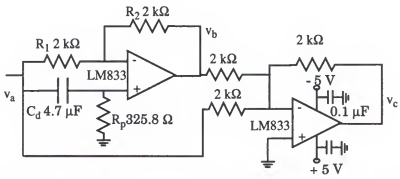


Figure 6-2 The circuit to generate balanced three-phase voltages.

as the reference signal and generates balanced three-phase voltages v_b and v_c from it. In balanced three-phase, v_b lags v_a by 120°; v_c leads v_a by 120°. Thus, v_c can be generated by a leading phase-shift circuit, and v_b is obtained just by adding v_a and v_c, as shown in Figure 6-2.

The phase-shift circuit in Figure 6-2 consists of one capacitor and three resistors. The resistors R_1 and R_2 decide the voltage gain that is one when they are equal. The resistor R_p and capacitor C_d determines the amount of phase-shift that is given by the following equation:

$$\phi_{lead} = 2tan^{-1}\left(\frac{1}{\omega R_p C_d}\right) \tag{6.1}$$

Given $C_d = 4.7\ \mu F$, $\omega = 2\pi(60Hz)$, $R_p = 325.8\ \Omega$, v_c leads v_a by

$$\phi_{lead} = 120^o \tag{6.2}$$

For a balanced three-phase system, v_b can be obtained by

$$v_b = -(v_a + v_c) \tag{6.3}$$

that is done by an inverted adder in Figure 6-2. The experimental waveforms are shown in Figure 6-3.

The three-phase line-to-line voltages are used to synthesize the six-step reference voltages v_1 and v_2 in the SVM. They are simply generated by subtracting two line-to-neutral voltages, as shown in Figure 6-4. Their experimental waveforms are shown in Figure 6-5.

The six-step signals S_{g1} - S_{g6} are used to assign the PWM signals produced by the LPWM to the six switches in the boost inverter, as shown in Fig-

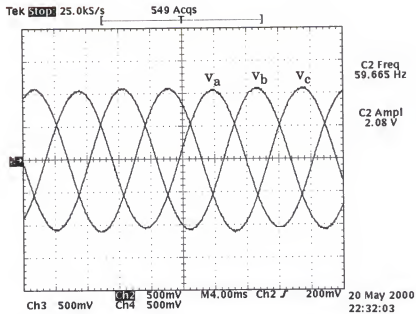


Figure 6-3 The experimental waveforms of three-phase reference voltages.

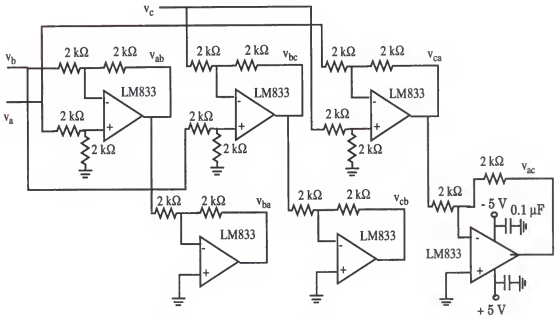


Figure 6-4 The circuit to generate three-phase line-to-line reference voltages.

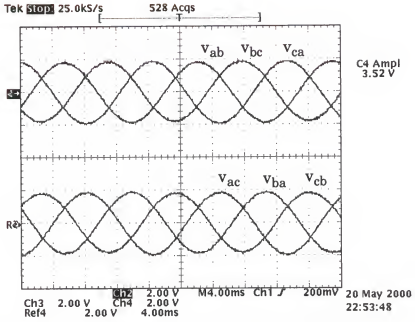


Figure 6-5 The experimental waveforms of three-phase line-line reference voltages.

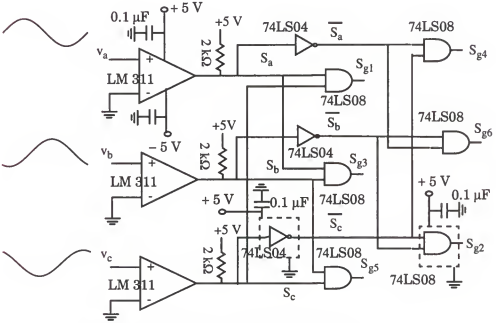


Figure 6-6 Six-step signal generator.

ure 6-1(a). S_{g1} - S_{g6} are generated by the circuit shown in Figure 6-6. By comparing three-phase voltages v_a, v_b, and v_c with zero volt, the circuits generate three digital signals S_a, S_b, and S_c that are in phase with v_a, v_b, and v_c, respectively, as shown in Figure 6-7. The six-step signals S_{g1} - S_{g6} are

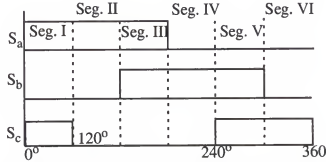


Figure 6-7 Signals S_1, S_2, and S_3 generated from three-phase voltages v_a, v_b, and v_c.

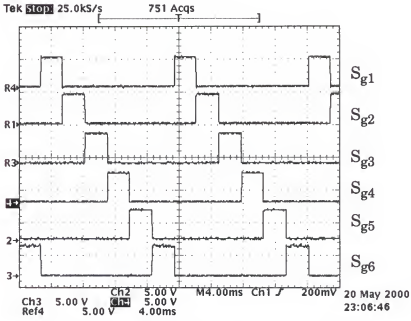


Figure 6-8 The experimental waveforms of six-step signals of S_{g1} - S_{g6}.

obtained from S_a - S_c by logic circuits, as shown in Figure 6-6. The experimental waveforms of six-step signals are shown in Figure 6-8.

The high-order LPWM employs the discontinuous reference voltage, v_1 and v_2, and input voltage V_g to determine the PWM signals S_1, S_2, and S_3, as shown in Figure 6-1(a). v_1 and v_2 are piecewise line-to-line reference voltages, the values of which are listed in Table 6.1 for the six steps of the SVM.

Table 6.1 The reference voltages v_1 and v_2 for six steps.

Steps	v_1	v_2
I	v_{ab}	v_{cb}
II	v_{ac}	v_{ab}
III	v_{bc}	v_{ac}
IV	v_{ba}	v_{bc}
V	v_{ca}	v_{ba}
VI	v_{cb}	v_{ca}

Table 6.2 The logic table of analog multiplexer CD4051.

C (S_c)	B (S_b)	A (S_a)	Output (v_1)	Output (v_2)
0	0	1	v_{ac}	v_{ab}
0	1	0	v_{ba}	v_{bc}
0	1	1	v_{bc}	v_{ac}
1	0	0	v_{cb}	v_{ca}
1	0	1	v_{ab}	v_{cb}
1	1	0	v_{ca}	v_{ba}

The relationship between steps and reference voltages in Table 6.1 can be implemented by analog multiplexers. The logic table of multiplexers is shown in Table 6.2, in which A, B, and C are input states of the multiplexer. The circuit implementation is show in Figure 6-9. The experimental waveforms of six-step voltages v_1 and v_2 are shown in Figure 6-10.

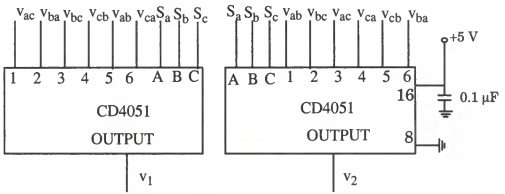


Figure 6-9 Analog multiplexers to generate reference voltages v_1 and v_2.

The high-order LPWM simulated in Section 4.5 of Chapter 4 is redrawn in Figure 6-11. The integrator shown in Figure 6-11 is implemented by an Op-Amp and two analog switches in the prototype circuit, as shown in Figure 6-12. The analog switch HI-201s is on when the control signal is low; it is off when the control signal is high. Thus, one inverter is needed to invert the control signal so that the switch is on when the external control signal is high; it is off when the external control signal is low. The operation waveforms of this integrator are shown in Figure 6-13. At the beginning of switching cycle, capacitor C is discharged by reset signal. The output voltage v_o of the integra-

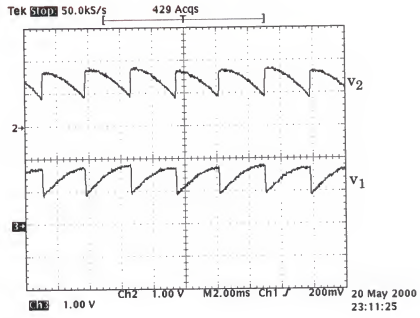


Figure 6-10 The experimental waveforms of six-step reference voltages of v_1 and v_2.

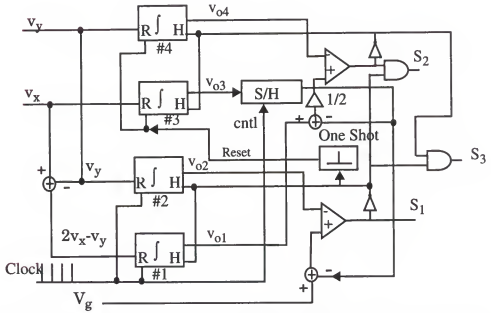


Figure 6-11 The high-order LPWM modulator used in the simulation.

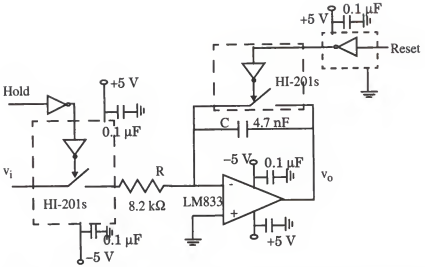


Figure 6-12 The integrator circuit with sample and hold.

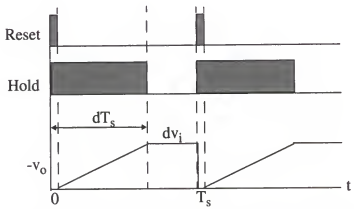


Figure 6-13 The operation waveforms of the integrator with sample and hold.

tor becomes zero. After reset, the integrator starts to integrate the input voltage v_i. The output voltage v_o is

$$v_o = -\frac{1}{RC}\int_0^t v_i dt \tag{6.4}$$

At the moment $t = dT_s$, the input signal v_i is disconnected from the integrator by the Hold signal, and the output voltage v_o will be held at

$$v_o = -\frac{1}{RC}\int_0^{dT_s} v_i dt = -\frac{dT_s}{RC}v_i = -dT_s K v_i \tag{6.5}$$

where v_i is assumed constant during each switching cycle, and K is the gain of the integrator. If time constant RC is designed equal to the switch period T_s, then,

$$v_o = -dv_i \tag{6.6}$$

The inputs to the integrators of the LPWM are six-step voltages v_1 and v_2, linear functions of control voltages generated by analog multiplexers in Figure 6-9. The input $2v_1$-v_2 is the linear combination of v_1 and v_2 that can be implemented by a simple subtractor, as shown in Figure 6-14 (a). The sample/

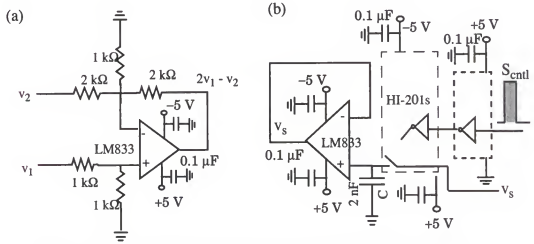


Figure 6-14 (a) The subtractor circuit; (b) sample and hold.

hold circuit in Figure 6-11 is implemented by one capacitor and one Op-Amp as shown in Figure 6-14 (b). When the sampling signal S_{cntl} is available, switch HI-201S is turned on. Capacitor C is charged to input voltage v_s. After the switch is turned off, this value will be held until next sampling signal is available. The prototype of the high-order LPWM is shown in Figure 6-15. The reset signal for the integrator #1 and #2 comes from the clock signal. Instead of the one-shot circuit to generate the reset signal for the integrators #3 and #4, the prototype circuit uses $\overline{Clock} \bullet S_1$ to generate the reset signal for them.

When there is a clock signal, the integrators #1 and #2 are reset; the value of integrator #3 is sampled by this signal and held in the S/H circuit for the calculation of PWM signal S_1. After the clock signal, two integrators on the bottom start to integrate their input signals until the output of integrator #2 reaches the input at the "+" pin of the comparator. At this moment, the PWM signal S_1 goes to zero, and the output of integrator #1 is held for the calculation of the PWM signal S_2. During the period S_1 is on, the two integrators on the top are kept reset, and S_2 is zero. As soon as S_1 becomes zero, these integrators start to integrate their inputs, and S_2 becomes one. When the output of integrator #4 equals the input of the comparator, the PWM signal S_2 goes to zero, and the output of integrator #3 is held for next calculation. The PWM signal S_3 is generated by $\overline{S_1} \bullet \overline{S_2}$.

The operation of the high-order LPWM is verified by the experimental results of the prototype circuit. Figure 6-16 shows the outputs of integrators in the high-order LPWM modulator; input and output waveforms of comparators

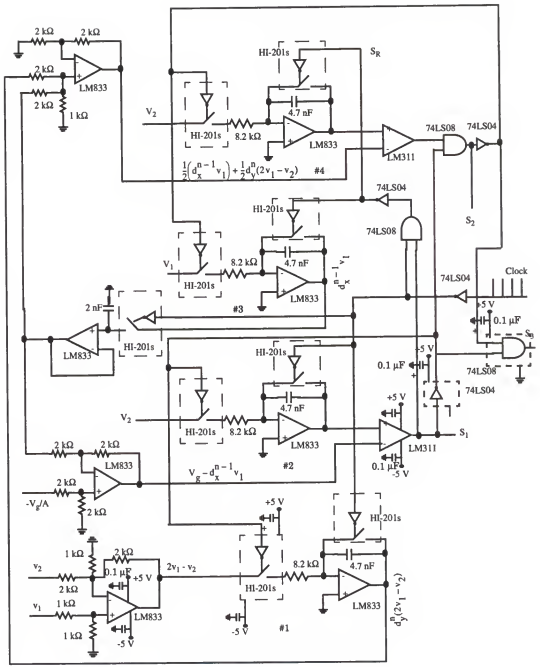


Figure 6-15 The prototype of the analog high-order LPWM for the three-phase boost inverter.

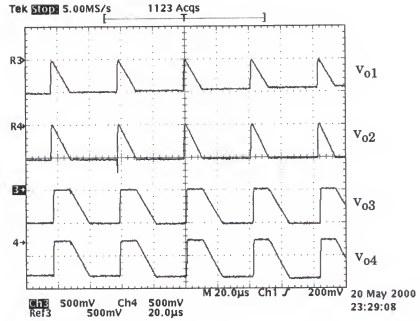


Figure 6-16 The experimental waveforms of the integrators of the prototype high-order LPWM.

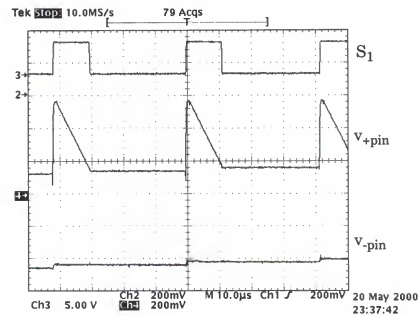


Figure 6-17 The experimental waveforms of the comparator for the PWM signal S_1.

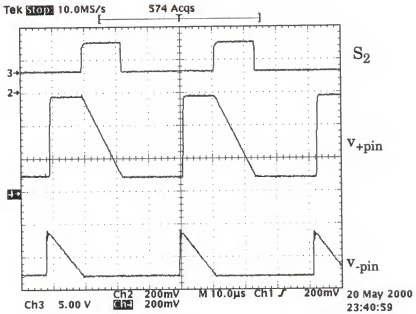


Figure 6-18 The experimental waveforms of the comparator for the PWM signal S_2.

are shown in Figure 6-17 and Figure 6-18, respectively. The output waveforms of the high-order LPWM are shown in Figure 6-19. All the waveforms agree with the analysis.

The output signals of the high-order LPWM, S_1, S_2, and S_3, are assigned to the six switches of the inverter by the gate-drive logic shown in Figure 6-20. The experimental waveforms of the switching signals for the six switches S_{11} - S_{23} are shown in Figure 6-21. After being averaged by low-pass filters, the duty ratios of PWM signals are obtained and shown in Figure 6-22. Obviously, in space-vector modulation, the duty ratios of switching signals are piecewise sinusoidal waveforms that agree with the discussion in Chapter 3.

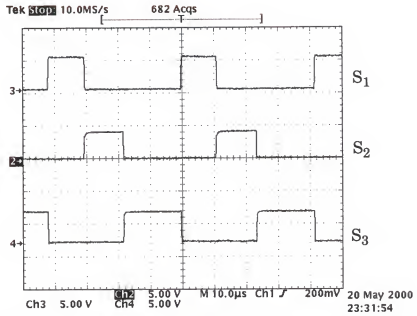


Figure 6-19 The experimental waveforms of the outputs of high-order LPWM.

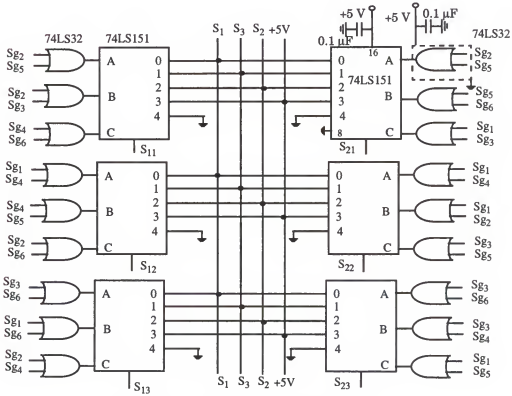


Figure 6-20 Gate-drive logic.

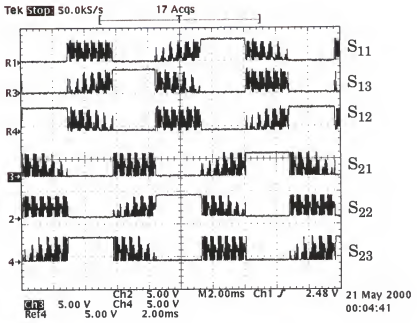


Figure 6-21 Experimental waveforms of PWM signals for the six switches in the inverter.

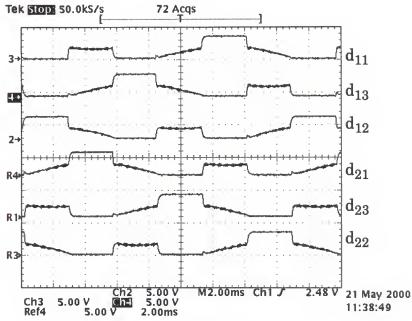


Figure 6-22 Experimental waveforms of duty ratios of PWM signals for the six switches in the inverter.

To drive MOSFETs in the inverter shown in Figure 6-1, signals S_{11} - S_{23} generated by gate-drive logic shown in Figure 6-20 need to be transferred from 5 V to 12 V by MOSFET drivers. To drive MOSFETs in the inverter that have floating gate and source, isolation circuits, such as opto-couplers, are required. The circuit that transfers signals S_{11} - S_{23} to MOSFETs and provides isolations is shown in Figure 6-23. MOSFETs M_{11} - M_{13} have floating

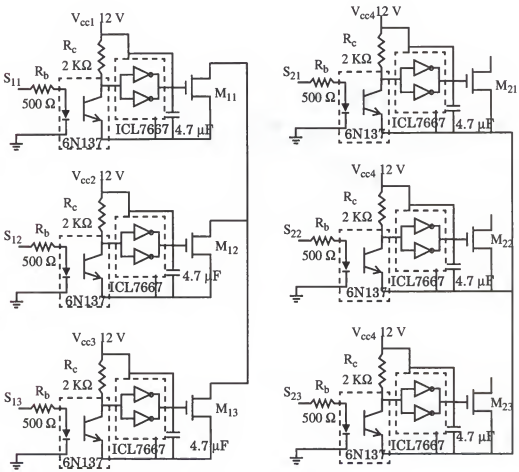


Figure 6-23 Opto-couplers and MOSFET drivers.

gate and source, thus, three separate power supplies, V_{cc1}, V_{cc2}, and V_{cc3}, are required to drive them, as shown in Figure 6-23. MOSFETs M_{21}, M_{22}, and M_{23} have the same ground, only one power supply V_{cc4} shown in Figure 6-23 is required to drive them. The allowed forward current of opto-coupler 6N137 is from 6.3 mA to 15 mA, so the resistor R_b in series with diode is designed to be 500 Ω (5 V/10 mA). The collector resistor R_c is designed to be 2 KΩ that gives on-state current 6 mA (the maximum value is 13 mA).

6.2 Experimental Results

The high-order LPWM developed in this chapter is used to control a three-phase boost inverter, as shown in Figure 6-1 (a). The reference voltage is given by

$$v_a = V_m \sin \omega t \tag{6.7}$$

The high-order modulator uses a portion of input voltage as its dc reference voltage and the value is given by

$$V_{gr} = \frac{V_g}{A} \tag{6.8}$$

According to Chapter 5, the output voltage is given by

$$v_{oa} = AV_m \sqrt{1 + (\omega RC)^2} \sin(\omega t - \theta) \tag{6.9}$$

where the phase is decided by

$$\theta = tan^{-1}(\omega RC) \tag{6.10}$$

Since the gain of the integrator K is not equal to the switching frequency due to the component errors, Equation (6.9) is modified by

$$v_{oa} = AV_m \frac{K}{f_s} \sqrt{1 + (\omega RC)^2} \sin(\omega t - \theta) \tag{6.11}$$

where f_s is the switching frequency. Therefore, the output voltages of the three-phase boost track the control voltages linearly. The amplitude is determined by the amplitude of the control voltage and other parameters such as the ratio of the input-voltage divider, load resistance, filter capacitance, and ratio between switching frequency and the gain of the integrator. However, all these parameters are independent of the operating condition of the inverter. There is a phase shift between the output and control voltages that is caused by the output capacitor.

The output voltages of the three-phase inverter measured at 600 W are shown in Figure 6-24; the output voltages measured at 1000 W are shown in Figure 6-25. Both measurement results show that the high-order LPWM modulator is able to generate low-distortion sinusoidal waveforms in the three-phase boost inverter.

Figure 6-26 shows inductor current, input voltage, control voltage, and output voltage. A phase shift between the control and output voltages exists due to the load resistor and filter capacitor. The value can be found:

$$\theta = \frac{1.16 \text{ ms}}{16.67 \text{ ms}} \bullet 360^o = 25^o \tag{6.12}$$

This value is quite close to its theoretical values decided by Equation (6.10):

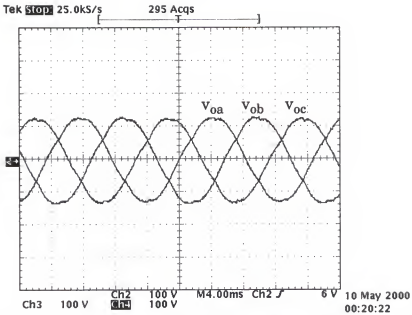


Figure 6-24 The three-phase output voltages of the inverter with R = 35 Ω

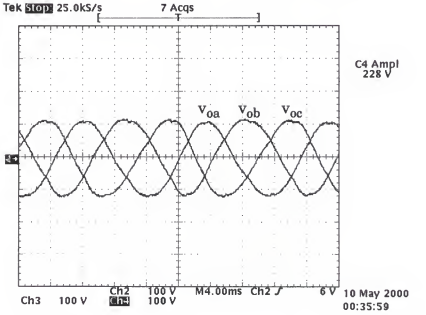


Figure 6-25 The three-phase output voltages of the inverter with R = 22 Ω

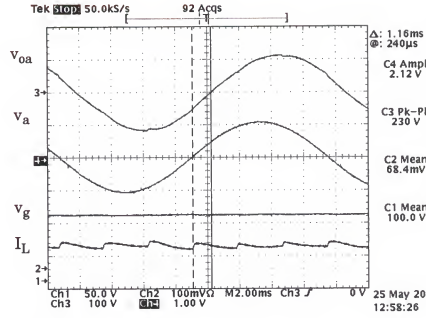


Figure 6-26 The output voltage, control voltage, input voltage, and inductor current. A = 100, K = 25.9 KHz, f_s = 24.5 KHz, R = 22 Ω, and C = 50 µF.

$$\theta = tan^{-1}(\omega RC) = 22.5^{o} \tag{6.13}$$

The amplitude of the output voltage is shown to 230 V/2 in the measurement. It is quite close to the theoretical value given by Equation (6.11):

$$V_{om} = AV_m \frac{K}{f_s}\sqrt{1+(\omega RC)^2} = 121\ V \tag{6.14}$$

where V_m is the amplitude of the control signal, 2.12 V/2 in the measurement. The difference between the measurement and theoretical value are due to power losses. The inductor current is dc with some ripples, and its average value is 6.84 A. The measured value and theoretical value are listed in Table 6.3 for comparison.

Table 6.3 Measured and theoretical output voltage and input current.

Variables	Measured Value	Theoretical Value
Voltage amplitude	115 V	121 V
Voltage phase	22.5°	25°
Input current	6.84 A	9.98 A

With the high-order LPWM control, the nonlinear three-phase boost inverter becomes a linear converter. The linearity of the converter is tested and verified by the prototype circuit. To test the linearity of the inverter, input voltage V_g is kept constant; the output voltage is measured for different control voltages. The curve of output voltage versus control voltage is shown in Figure 6-27. It is tested under the condition of V_g =50 and A =40.

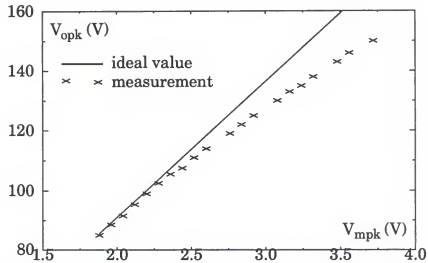


Figure 6-27 The linearity of the three-phase boost inverter controlled by the high-order LPWM.

The high-order LPWM modulator has good line voltage regulation. This is because any change of input voltage V_g will make duty ratio change in the same direction through the LPWM modulator. Therefore, the output voltage, inversely proportional to the duty ratio, can be kept constant. To test the line voltage regulation of the modulator, control voltage is kept constant; the output voltage is measured for different input voltages. The curve of output voltage versus input voltage is shown in Figure 6-28. It is tested under the condition of V_{mpk} =2.28 V and A = 53. When input voltage is varied from 45 V to 85 V, the steady-state line voltage regulation is in the range of 7%.

The efficiency of the inverter is measured, as shown in Figure 6-29. The switching waveform V_{gs} and V_{ds} of one MOSFET are shown in Figure 6-30. The voltage across the inductor is shown in Figure 6-31. Finally, the picture of

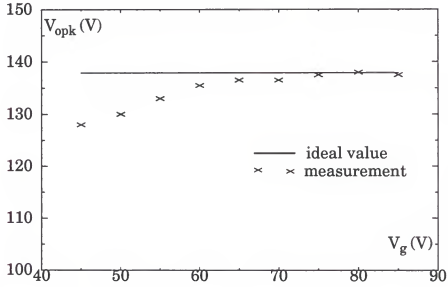


Figure 6-28 The input voltage regulation of the high order LPWM.

the prototype circuit is shown in Figure 6-32. The pictures of the high-order LPWM modulator is shown in Figure 6-34. The top views of the reference circuit and gate-drive logic are shown in Figure 6-33. The top view of the three-phase boost inverter is shown in Figure 6-35.

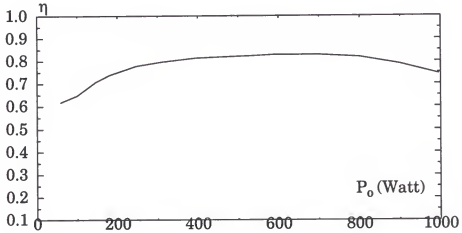


Figure 6-29 The efficiency of the prototype three-phase boost inverter.

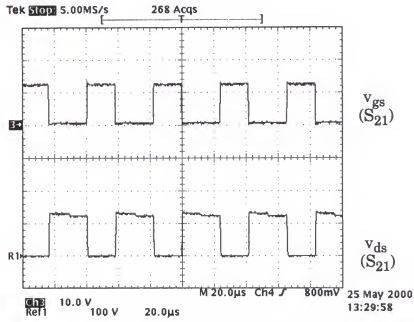


Figure 6-30 The switching waveforms of a MOSFET in the inverter.

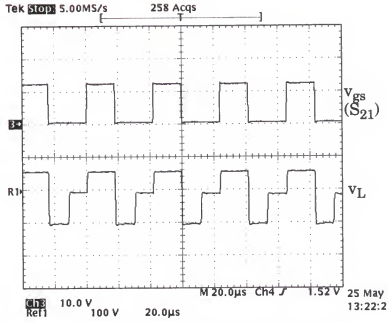


Figure 6-31 The waveform of the voltage across the inductor and gate signal of one MOSFET.

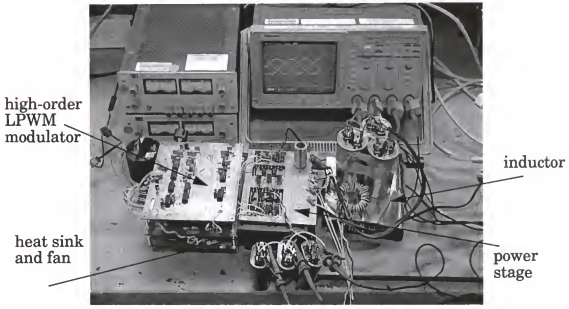
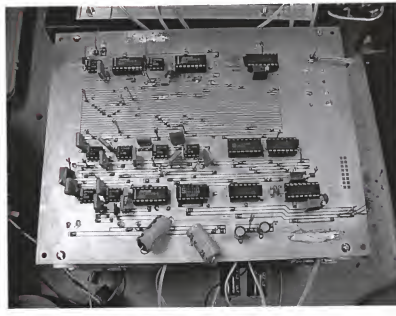
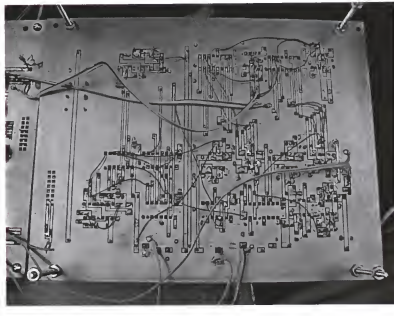


Figure 6-32 The picture of the prototype circuit.

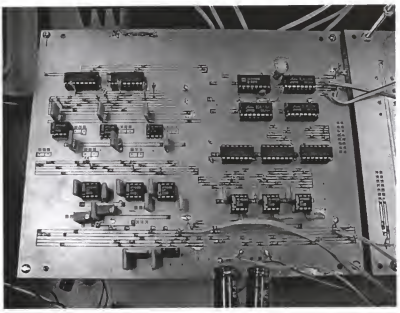


(a)

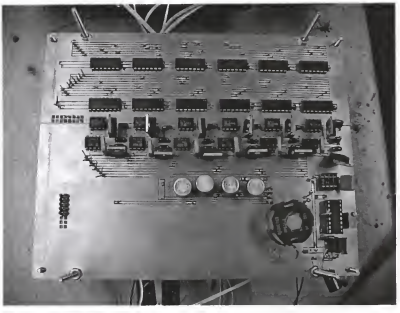


(b)

Figure 6-33 (a) Top view of the high-order LPWM modulator; (b) bottom view of the modulator.



(a)



(b)

Figure 6-34 (a) Top view of the reference circuit; (b) top view of the gate-drive logic.

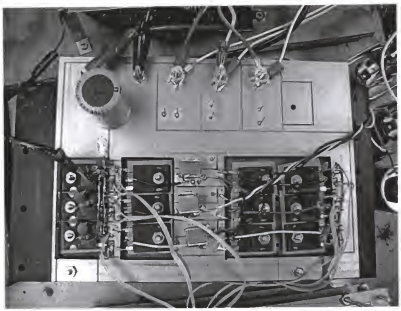


Figure 6-35 Top view of the three-phase boost inverter.

6.3 Practical Issues in Experiment

To make the test system work, several practical issues need to be considered, including component layout and common-mode noise. In component layout, a big current loop should be avoided because the big loop is associated with increased inductance. When there is di/dt noise around this loop, it will introduce a voltage determined by Ldi/dt. This voltage generates a spike in the signal, and it could make false operation in circuits. This situation is illustrated in Figure 6-36(a). A better layout is shown in Figure 6-36(b). To prevent signals from interfering each other, we should connect power paths of different components to ground separately. A layout for several signals sharing a power path is illustrated in Figure 6-37(a). In this layout, a noise associated with one

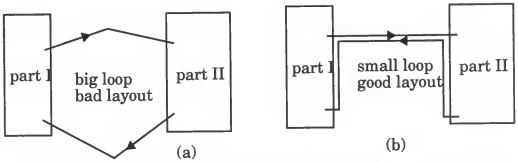


Figure 6-36 (a) Layout with a big loop; (b) improved layout with small loop.

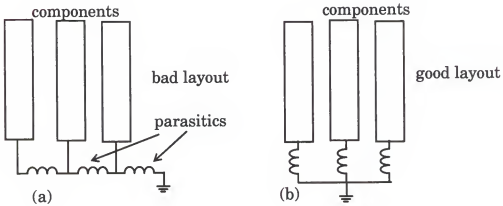


Figure 6-37 (a) Layout with a common ground line; (b) improved layout without ground sharing.

part would be shared by other parts. The better layout is shown in Figure 6-37(b), in which power paths are connected with ground by separate lines. To prevent power noise caused by high di/dt and parasitic L or dv/dt and parasitic C from contaminating control signal, we need to separate power and signal paths/grounds. Signal ground is connected to power ground is shown in Figure 6-38(a), in which parasitic L would introduce voltage spike into control signal.

A better layout is shown in Figure 6-38(b), in which signal path is directly connected to the source of power MOSFET.

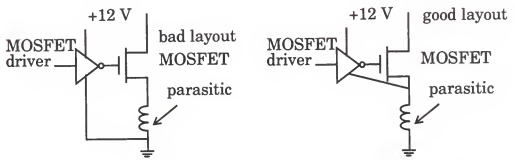


Figure 6-38 (a) power and signal share ground; (b) power and signal grounds are separated.

The test system consists of four circuit boards. There are signal connections among these boards. Each signal path should leave one circuit board and arrive another board together with its return path, as shown in Figure 6-39.

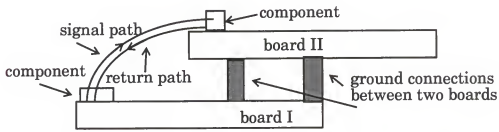


Figure 6-39 Signal connections between two circuit boards.

In general, the bottom line for layout is to keep the layout small and neat. Each current path and its return should be clearly identifiable and run parallel, in close proximity.

Common-mode current are shown in Figure 6-40(a) that flow in both signal path and its return path in the same direction. they generate common-mode noise and contaminate reference signals in the experiment. PWM signals generated from these contaminated reference signals are distorted, and would not operate the inverter correctly. The technique used to reduce com-

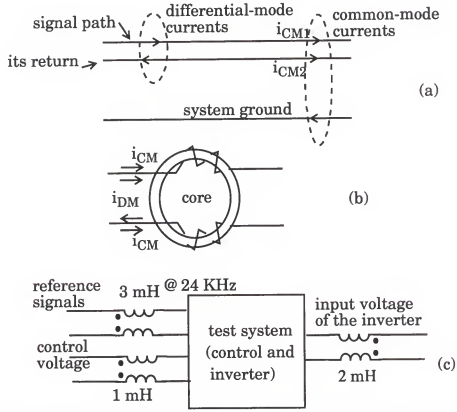


Figure 6-40 (a) common-mode currents; (b) common-mode filter; (c) test system showing three common-mode filters.

mon-mode noise in this experiment is to add common-mode filters to the reference signals. The common-mode filter is constructed just by wrapping signal and its return wires on the same magnetic core, as shown in Figure 6-40(b).

Since two inductors formed by signal path and its return path are on the same core and have the same turns, common-mode currents are forced to be equal. The same common-mode filters can be added to control voltage lines, and input power lines of the inverter. The system with common-mode filters is shown in Figure 6-40(c). Inductor values of common-mode filters used in the experiment are also shown in Figure 6-40(c).

Components used in the experiment are listed in Table 6.4. Output voltages of the inverter are 60 Hz sinusoids, thus, AC capacitors are used in the output of the inverter. The package of MOSFETs and diodes are TO-247 that is easy to be mounted on heat sinks by metal screw because there is no metal contact around the hole of the package. Analog switch HI-201S is very fast switch with t_{on} = 30 nS and t_{off} = 40 nS. It is used to reset capacitor in integrators of the LPWM at high switching frequency. Analog switch CD4051 is slower than HI-201S. It is used to generate six-step reference voltages. Operational amplifier LM833 has low distortion (0.002%), low offset voltage (0.3 mV), thus, it is very suitable for reference voltage circuit. It also has a wide bandwidth (15 MHz) without increasing external components or decreasing stability, thus, it is suitable for integrators in the LPWM. LM311 is used as zero-cross detector in the reference circuit shown in Figure 6-1 and voltage comparator in the LPWM shown in Figure 6-15. This devices are much less prone to spurious oscillations. Offset balancing and strobe capability makes LM311 easy to use in the experiment. High speed and current output of ICL7667 make it very suitable to drive MOSFET. In the experiment, two

devices inside one package of ICL7667 are paralleled to increase its driving capability.

Table 6.4 Components used in the experiment.

Component	Type
Inductor	3 mH Magnet Tek C-59U
Capacitor	Mallory (50 μF/370 Vac/60 Hz)
MOSFET	IRF360 (400 V, 20 A, 0.2 Ω)
Diode	MUR3060 (600 V, 30 A, 1.7 V)
Inverter power source	Sorenson DCR150-15A
OP AMP	LM833
Comparator	LM311
Analog switch	HI-201S
Analog multiplexer	CD4051
MOSFET driver	ICL7667
Opto-coupler	6N137
Digital multiplexer	74LS151
Inverter	74LS04
AND gate	74LS08
OR gate	74LS32
Voltage regulator	UA7805
Voltage regulator	UA7905

CHAPTER 7
SUMMARY AND CONCLUSION

This study shows that the three-phase PWM converters have nonlinear relationships between the control and output voltages when they are controlled by the conventional analog SPWM or SVM modulators. Some sophisticated analog circuits may employ analog multipliers/dividers to compute the switching instants for three-phase converters to implement linearization. However, the complexity of the resulting circuitry makes them impractical. The first-order linearizing PWM circuit uses integrators to compute commutation instants to linearize the control-to-output relationship for dc-dc converters or single-phase inverters. The first-order LPWM can also be used to control three-phase converters. However, as indicated in this thesis, the inputs to the integrators of the first-order LPWMs could be nonlinear functions of control voltages and must use analog multipliers/dividers.

A high-order linearizing PWM is developed in this thesis. It is able to make the output voltages of the three-phase PWM converter track the control signals linearly even in the nonlinear topologies. Instead of multipliers/dividers, the high-order LPWM uses only integrators with the reset, and sample/hold to compute the switching instants for the switches. The inputs to the integrators are linear functions of the control and state variables. The key to

implement the high-order LPWM modulator is the assumption that the duty ratio in the current switching cycle approximately equals that in the previous cycle. This assumption is true because the control signal is much slower than the switching frequency in practice. The analog high-order LPWM is simple and easy to use.

The general procedure of the synthesis of the high-order LPWM modulator for balanced three-phase converters is developed. The modulator is synthesized from the switching-function averaging (SFA) equations of the three-phase PWM converter. In this thesis, the derivation of SFA state-space equations is simply done by inspection and application of definition of circuit elements, Kirchhoff's law and other electrical principles without probing into topological details of the converter. The set of SFA equations can be transformed into an equivalent circuit in the *abc* coordinates to make simulation more efficient.

The circuit-oriented analysis technique is developed for balanced three-phase PWM converters. All the three-phase components, including PWM switches, sources, and passive components, are modeled in the *ofb* coordinates. After three-phase components are replaced by the *ofb* models, the time-variant three-phase circuit is transformed into a time-invariant equivalent circuit that makes analysis and design much easier. The model of the high-order PWM is also developed. It is useful to analyze the LPWM-controlled converter and evaluate time delay caused by sampling effects.

The synthesis procedures and analysis theories for the high-order LPWM and balanced three-phase PWM converters are demonstrated and simulated through a three-phase boost inverter in this thesis and checked with an experiment. A prototype 1 kW, 24 kHz three-phase boost inverter is used to test the high-order LPWM implemented by analog circuits. The experimental results agree with the simulation and the analysis. It is shown that the output voltages of the three-phase boost inverter can track the control voltages linearly with good sinusoidal waveforms. The disturbance of dc input voltage can be reduced in the output voltages, and line voltage regulation is improved. The analog circuits of the high-order LPWM modulator is simple and can be implemented easily.

In conclusion, the three-phase PWM converter can be linearized by the high-order LPWM modulator that uses integrators with the reset, and sample/hold to compute commutation instants. The inputs to the integrators are linear functions of control voltages. With the high-order LPWM control, the output voltages can track the control signals linearly with good waveforms, and the disturbance from the input voltage can be reduced. The control is stable, and analog implementation is simple. Time delay caused by sampling effects of the high-order LPWM is small because of high switching frequency, and it can be neglected in the design. The method of synthesis and analysis in this dissertation are general methods that can be applied to other three-phase topologies.

The high-order LPWM and the analysis techniques in this thesis are developed for the balanced three-phase converter. How to deal with the unbalanced three-phase or multi-phase systems is still confusing. The large-signal and small-signal models of the converter and modulator are derived in this thesis, but how to use these models to implement close-loop control still needs more time and effort. The prototype modulator is implemented by discrete analog components that consume a relatively large board area and need time to make it work. It is hoped that the modulator can be integrated in the future. This thesis is just a small step in a long journey. More challenging work lies ahead requiring more time, effort, and innovative mind.

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I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Khai D. T. Ngo, Chairman
Associate Professor of Electrical and Computer Engineering

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